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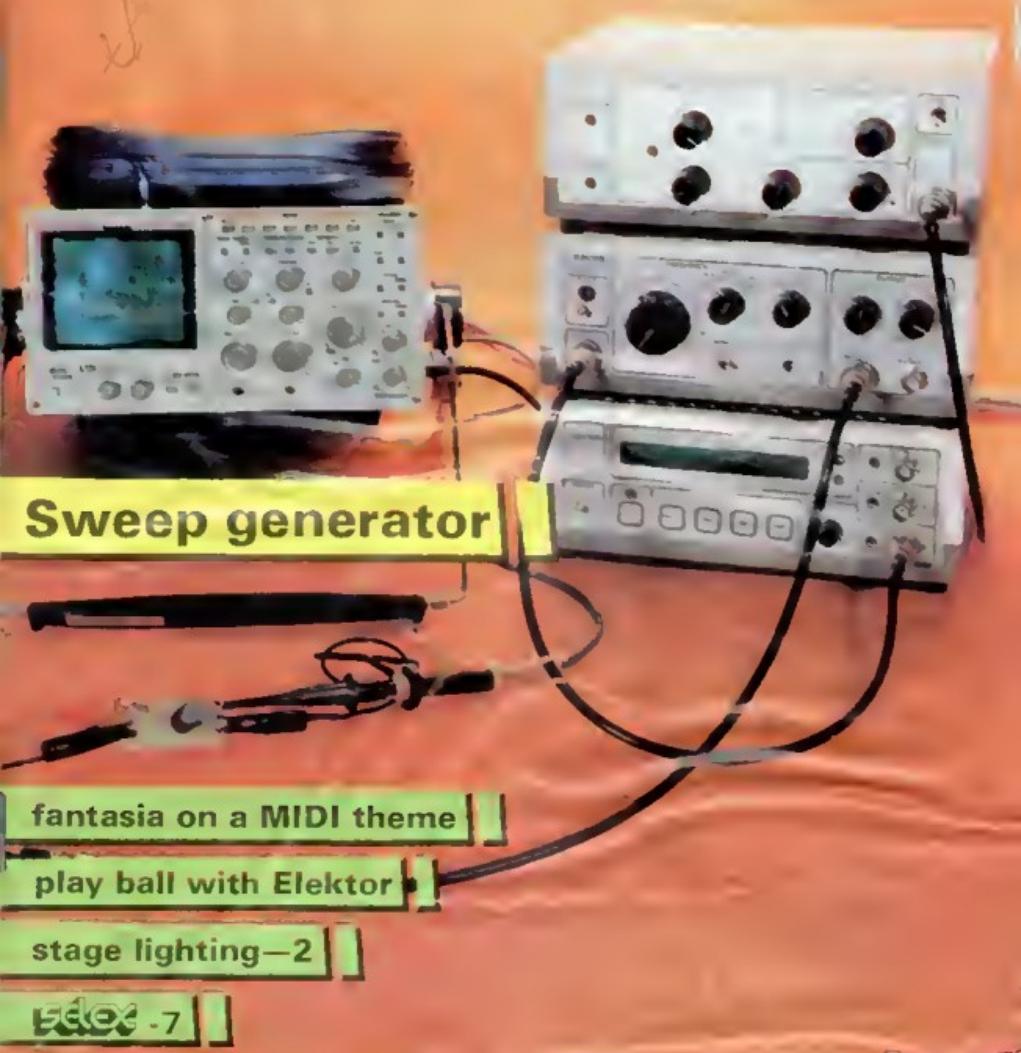
December
1985

elektor

INDIA

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electronics



Sweep generator

fantasia on a MIDI theme

play ball with Elektor

stage lighting—2

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This month's cover shows a typical test set-up for the sweep Generator described on pp. 12-26 & 12-32. Also in the picture are the Function Generator and the uP-Controlled Frequency Meter described in the January and February 1985 issues of Elektor India respectively.



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To all our readers: thank you!

In this, our last message to you in 1985, we want to express our heartfelt thanks to all of you who have loyally supported us throughout the past year. We never forget that it is essentially you who keep this wonderful magazine of ours going. We, for our part, will continue to do our utmost to give you the best we can from the fascinating world of electronics. There will always be something of interest for all of you, whether you work professionally in electronics, or are merely interested in it for your leisure hours: projects for home construction; articles of an informative nature on the electronics of today and tomorrow; news and views; and, of course, such regulars as New Products and New Literature. Our particular aim is to offer a better balance between articles dealing with construction projects and those of a descriptive and informative nature. None the less, construction projects will continue to form the nucleus of the magazine. Furthermore, we are planning a Readers Letters column to enable you to express an opinion, or tell your fellow readers about an interesting or unusual aspect in the field of electronics, or to exchange ideas with us or other readers. Again, we will be grateful for your support in this. There has, unfortunately, been one aspect of our services that has suffered through the restructuring of the editorial department and other changes that have taken place during the past twelve months: our response to your letters. Some of you must at times have felt a sense of utter frustration, if not of downright anger. For this, we apologize. At the same time, we would assure you that we are slowly coming to grips with the backlog, and hope to be back to normal by the beginning of the new year. Finally, to round off this message of goodwill, all of us at Elektor India wish you a Merry Christmas and a Happy New Year.

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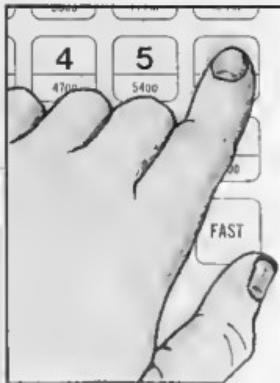


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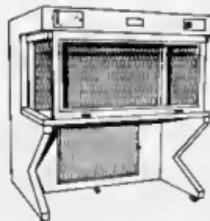
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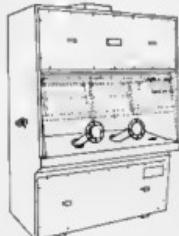
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EEPROMS

Excel Microelectronics Inc., believed to be the pioneering company in making electrically erasable memory chips, is considering a proposal to set up a subsidiary in India, according to reports. Mr B K Marya, an India-born American citizen, who is president of the company, is quoted as saying that he is interested in India primarily for two reasons, namely cheap labour and highly qualified technical talent. The Indian subsidiary will be entrusted with the job of silicon wafer fabrication which can finally be converted into "Electrically Erasable and Programmeable Read Only Memory" (EEPROM) chips. Since the Indian market was not yet ready for using the EEPROM chips, the company would have 100 per cent buy back arrangement.

POWER ELECTRONICS

A national seminar on the role of electronics in the power sector, held recently at Delhi, has adopted a set of recommendations which have been submitted to the government for consideration.

The seminar organised by the National Council for Power Utilities and "Urja", a journal devoted to energy, called upon all power generating and distributing organisations to integrate electronics in their power distribution and monitoring systems and in their communication networks.

The seminar opined that the power sector should go for digital communication and low-cost satellite terminals to be used at power stations and at large grid substations to transmit data. An action plan for the implementation of an integrated communication system for power stations management should be drawn up at the earliest, the seminar concluded.

For adopting computerised and microprocessor-based distribution systems by the power utilities in a phased manner, it has been suggested that one 210 MW unit and one 500 MW unit should be earmarked as units on which new electronics and computer applications could be tried out for their usefulness under Indian conditions.

TCIL DIVERSIFIES

Telecommunications Consultants India Ltd (TCIL), an organisation under the Union ministry of communications, is poised for making feasibility studies for the introduction of cellular mobile radio communication system, view data, yellow page service and office automation.

electronics scene

The organisation is currently carrying out a feasibility study on digital transmission, telemetry and telecontrol for oil pipeline and gas pipeline system. It is also setting up a computer network on an experimental basis for exchange of information among computers in three cities - Delhi, Bombay and Madras.

TCIL, which has so far been operating in conventional fields like switching, transmission and satellite communication, has recorded the highest net worth growth rate among all public sector undertakings, according to Mr. M. P. Shyka, chairman and managing director of the company.

Mola saves British Telecom £10 million a year

A £100 device that could save about £10 million a year in maintenance costs has won its inventor first prize in British Telecom's New Ideas Competition.

Ernie Huggins, a 59 year old assistant executive engineer, worked for two years in his spare time to conceive the Mole, an electronic locator which can pinpoint faults in underground cables simply and accurately. It reduces the number of holes that have to be dug for each fault from five to two, saving money and reducing disruption to the public.

There are already 3000 Moles in use by British Telecom throughout the UK, and licences are being arranged for its manufacture and sale throughout the world.

Runner-up was Jed Isbell, a 29 year old manager from London, who devised a testing system that will make British Telecom's Pocket SwitchStream network even more reliable.

Highly commended were Perry Bebbington and Peter Moseley, both technical officers from Nottingham, for an idea that enhances the compatibility between the Monarch and Herald electronic switchboard systems.

Database helps choose computers

A computerized database, which allows any company considering computerization to have a specification of their business requirement to be fed into the system and matched against existing available systems, is being offered to computer consultants throughout the world under licensing agreements.

The database, Computerscan, is a fourth generation system that is able to give reasoned, intelligent answers about information stored in its

memory. It was developed by Atlas Computer Consultancy (UK) Limited of Preston, Lancs, and has been tried successfully by many companies in Britain.

The database has details of over 3000 suppliers, incl. 60 000 application software packages. This information greatly exceeds that which a computer consultant could analyse during research.

In addition to licensing agreements, the company has undertaken a period of investment to enable a worldwide consultancy service to be offered from its headquarters. Assistance has already been given to the UN in Geneva, as well as to organizations in New Zealand, Nigeria, Dubai, and Australia. (LPS)

Thick film in cars

The new Granada Scorpio, the latest model from the Ford Motor Company, owes one of its smallest, but most vital parts to Swindon-based BICC-CITEC. This company has designed and manufactured the thick-film fuel tank sander resistive element which indicates not only the amount of petrol in the tank, but also enables the miles per gallon ratio to be calculated by the in-car computer.

The element consists of a thin ceramic tile on which the resistive track is screen-printed with a specially devised cermet ink that is capable of withstanding both the corrosive environment of blended petroleum and the constant track wear caused by the wiper.



BICC-CITEC has been developing sander elements for Ford for three years, beginning with the launch of the Sierra, and currently produces around 250 000 elements a year for the Granada, Sierra, and top-of-the-range versions of the Orion and Escort models.

electronics scene

CHIPRIGHT ACT

Any invention needs a protection from illegal imitations and the interest of the inventor is safeguarded by what is known as the Patent law. In the computer industry, the piracy of computer software programmes threw up a new challenge as the product sought to be protected here is not a design of a watch or a television but an intellectual thought. Legal provisions have been evolved in countries like the USA to check the software piracy.

Of late, semiconductor integrated chips have also become a victim of intellectual plagiarism and the original designer is left with little profits as his designs are proliferating illegally in the hands of *ecce* copiers. The ICs play such an important role in various fields that experts call it the "crude oil of electronic industry" to signify its economic potential.

The major part of development cost of new ICs goes for the enormous amount of time and effort spent on designing the circuit layout. As the degree of integration of thousands of elements together on a tiny semiconductor substrate progresses, the developmental costs will also increase. At the same time, if competitors copy the circuits without incurring the developmental costs, the return for the original designer will dwindle and also hamper his interest in the work.

Until recently, neither the Copyright Act nor the Patent Act adequately protected the original designs of the ICs. In late 1983, the Japan-US working group on high technology industries observed that "both governments should recognise that some form of protection to semiconductor producers for their intellectual property is desirable to provide the necessary incentives for them to develop new semiconductor products". The group concluded that "both governments should take their own appropriate steps to discourage the unfair copying of semiconductor products and the manufacturing and distribution of unfairly copied products".

The United States enacted a new Semiconductor Chip Protection Act in 1984. Japan, the second largest supplier of ICs in the world, has also followed suit. A few months ago, the Japanese ministry of international trade and industry prepared a bill

and the Act concerning the Circuit Layout of Semiconductor Integrated Circuits was passed in the Diet. The Act will come into effect on a date to be announced by the Japanese government.

The Japanese Act, though similar to the American Act, has three differences. Protection is extended to all persons, regardless of nationality, whereas the US law is based on "reciprocity"; protection begins on the date of registration under the provisions of the Act and not from the date of first commercial exploitation, and infringement can result in criminal punishment.

Under the Japanese Act, the subject of protection is called "circuit layouts" which is described as "mask work" in the US law. The exclusive rights acquired by the creators include manufacturing, transfers, leases, exhibitions and imports of any product incorporating the original layouts. The right holder can demand an injunction and compensatory damages for any infringement which is punishable by imprisonment up to three years or a fine not exceeding one million yen.

These rights are not absolute. Independent development, which is different from imitation, of an identical layout will be granted a similar copyright. The Act provides protection for ten years.

RAJIV'S KEYBOARD

A local area computer network has been designed and installed in the office of the prime minister, Mr. Rajiv Gandhi, which is being operated by the prime minister himself. As a consequence, all senior officers from the level of additional secretaries to the level of section officers are now learning to use computers programming. Dr. N. Sneshegiri, additional secretary to the department of electronics, revealed this information in his keynote address to the two-day national conference on computers for productivity and quality organised by the Pune Chapter of Computer Society of India.

The proposed installation of supercomputers at New Delhi, Pune, Hyderabad and Bhubaneshwar will help eliminate the "ad hocism" rampant in various Union ministries, particularly in formulation of policies and programmes, Dr. Seshagiri said. With the supercomputer net work, it would be possible to have

information in analytical forms which can be called on the video screen with the touch of a button. The supercomputer in New Delhi, which is ready to come on line any moment, will serve the entire northern region. Supercomputers in Pune and Bhubaneshwar would be ready by March, 1986 and the one at Hyderabad by May, 1986, according to Dr. Seshagiri.

The supercomputers would be connected to 430 small computers, one in each district headquarters, throughout the country via earth stations and the satellites INSAT-1A and INSAT-1C. The entire country is expected to be covered by this network by 1987. This network will provide the data base for the central and state governments. This network information collected by various agencies like the National Sample Survey Organisation, Central Statistical Organisation, departments of rural development, agriculture, education, health etc. etc., would be analysed at each hierarchical level and stored for retrieval in the supercomputer network.

India was in a position to design complex civilian and mechanical parts, off-shore drilling platforms, launching pads for rockets and even shipbuilding with the aid of software procured from Norway, it was pointed out.

Mr Arun Firedia, managing director of Kinetic Honda Motor Company, who inaugurated the conference stressed the indispensability of computers for modern industry. Computer techniques could be used to design fuel efficient automobile engines, he added, for an example.

SPENCER COMPUTERS

Spencer and Company, Madras, better known for their soda, having diversified into a variety of fields like pharmaceuticals, shrimp export, department stores and so on, have now entered the computer field. The company has taken up the sole selling agency of the French computer firm Honeywell Bull. The company proposes to take up assembly and manufacture of small computers with commercial applications and process controls and negotiations were in progress with three American firms for a joint venture in this arena. Simultaneously, Spencer would venture into a project for the development and export of computer software.

a star for Christmas

by D Folger

The time of the year has arrived again (doesn't it come quicker and quicker?) when most of us are frantically racking our brains trying to decide on suitable presents. If you are in that position, this little Christmas Star may solve one of your problems. It is not a complicated circuit, as its appearance is obviously of far greater importance than its technical ingenuity.

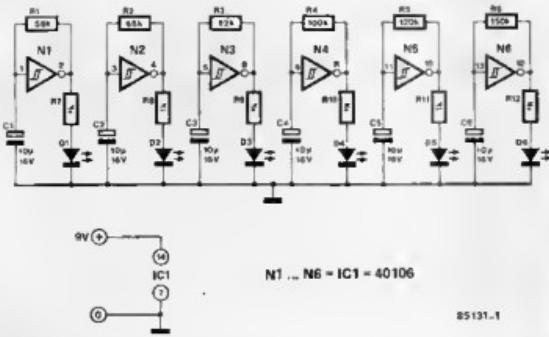
It sometimes appears as if there are light-emitting diodes all around us, and certainly they have gradually replaced filament bulbs and neon lamps in all sorts of applications. Since these tiny components are now available in five different colours (red; amber; yellow; green; and blue), they are eminently suitable for use in ornamental lighting. When LEDs are arranged to light in flashes, rather than constantly, they can be made into very attractive, eye-catching ornaments.

The circuit consists essentially of six relaxation oscillators as shown in Fig. 1. Because the feedback resistors have a different value in each of the oscillators, the width and rate of the generated pulses will vary. Each LED lights for a time dependent upon the width of the relevant pulse, while the frequency at which it will be switched on and off is deter-

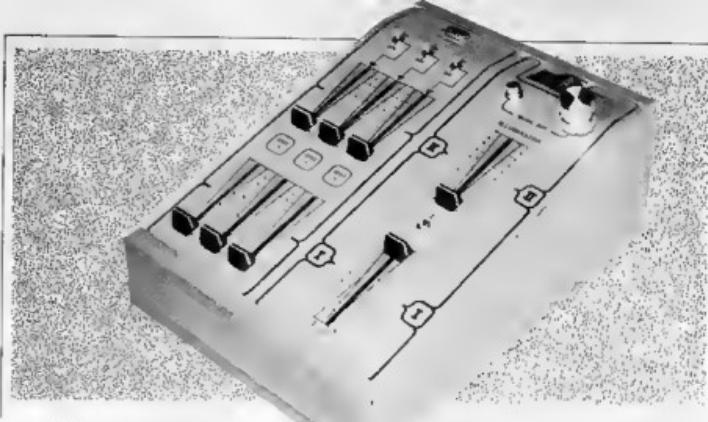
mined by the relevant pulse rate. The circuit is powered by a 9 V Type PP3 battery or equivalent. The average current drawn amounts to 20 mA.

Construction

An example of how the Christmas Star may be constructed is shown in the photograph. It is recommended to use an IC socket and not to solder direct onto the IC pins. The component terminals may be stiffened by encasing them in araldite or simply with some suitable sleeving. An on-off switch was considered unnecessary, since it is a simple matter to connect and disconnect the supply with the battery clip. The colour of the LEDs used is left to your own imagination and taste.



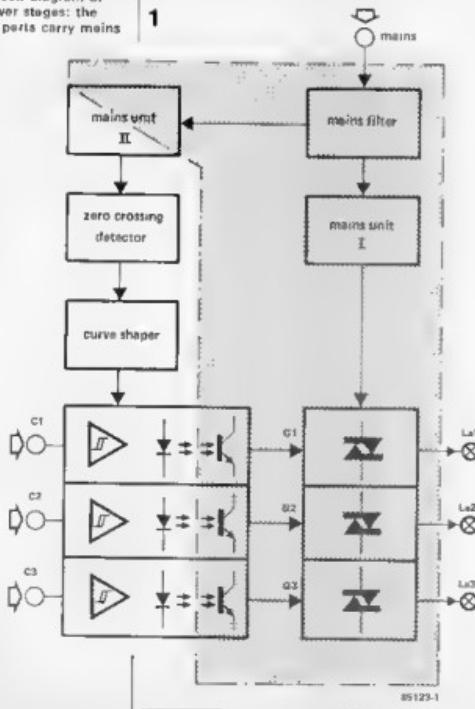
by A Sevriens



stage lighting 2

The power stages for the stage lighting form a completely independent unit with voltage-controlled inputs. For a number of reasons, it should be contained in its own enclosure. The control cable from the control panel can then easily be up to 100 feet long, so that the power unit may be installed close to the lighting, i.e., between the mains supply and the flood lights, spot lights, or whatever other lights that may be used.

Fig 1 Block diagram of the power stages: the shaded parts carry mains voltage



Block schematic

To ensure first-class performance, filters are provided between the mains supply and all electronic circuits as shown in Fig.1. This obviates the possibility of any mains interference reaching the electronic circuits, and also of any feedback from these circuits onto the mains supply. The mains filters are, of course, additional to the decoupling already provided in the electronic circuits. Mains unit I provides the power needed for the control of the triac stages which are shown here in simplified form.

Mains unit II provides the power for the control circuits and isolates the control panel from the mains. The zero crossing detector and curve shaper ensure that the triacs are fired in a manner which ensures that the brightness of the lighting varies in linear proportion to the setting of the relevant slide potentiometer at the control panel. The voltages provided by the potentiometers are applied to inputs $C_1 \dots C_3$.

The role of the comparators will be discussed later.

The opto-isolators isolate the control signals from the gates of the triacs.

Circuit description

The mains voltage is applied to the mains transformer via a 15 A mains filter. This allows a maximum total dissipation of 3600 W, i.e., 1200 W per lamp channel. None the less, more power may be provided: this will be reverted to later.

Mains unit I of Fig.1 consists of T_{R1} , D_1 , D_2 , and C_1 . The voltage across C_1 is about 10 V, and the maximum permissible current is 500 mA, which is more than adequate. It is important to note that the negative terminal of C_1 is connected to the mains!

Zero crossing

The control panel provides the power stages with direct voltages, on the basis of

which the latter have to ensure a certain brightness of the lighting. This means that these direct voltages have to be converted into appropriate phase gating angles. This is only possible if first the exact moment that the mains voltage passes through zero is established: this moment is used as a reference point. The determination of it is carried out by T_4 and monostables MMV_1 and MMV_2 .

The operation is clear from the timing diagram in Fig.3. Curve 1 represents the mains voltage, and curve 2 the rectified output of the mains transformer. The pulses in 3 indicate that T_4 switches on as soon as the voltage at its base exceeds 1.2 V. A pulse appears at the collector of this transistor when its base potential drop below 1.2 V. This pulse coincides with the mains voltage passing through zero.

Fig.3 (4) shows the output signal of MMV_1 . This multivibrator is arranged in such a way that it is triggered by the leading edge of the pulse provided at the collector of T_4 ; it can-

not be triggered again before it has been reset. The duration of its quasi-stable state can be set between 8 and 11 ms with P_1 . MMV_2 is triggered by the trailing edge of the pulse output by MMV_1 . The period of its quasi-stable state is fixed at 0.5 ms — see Fig.3 (5), from which it is clear that the negative pulse output by MMV_2 coincides exactly with the mains zero crossing.

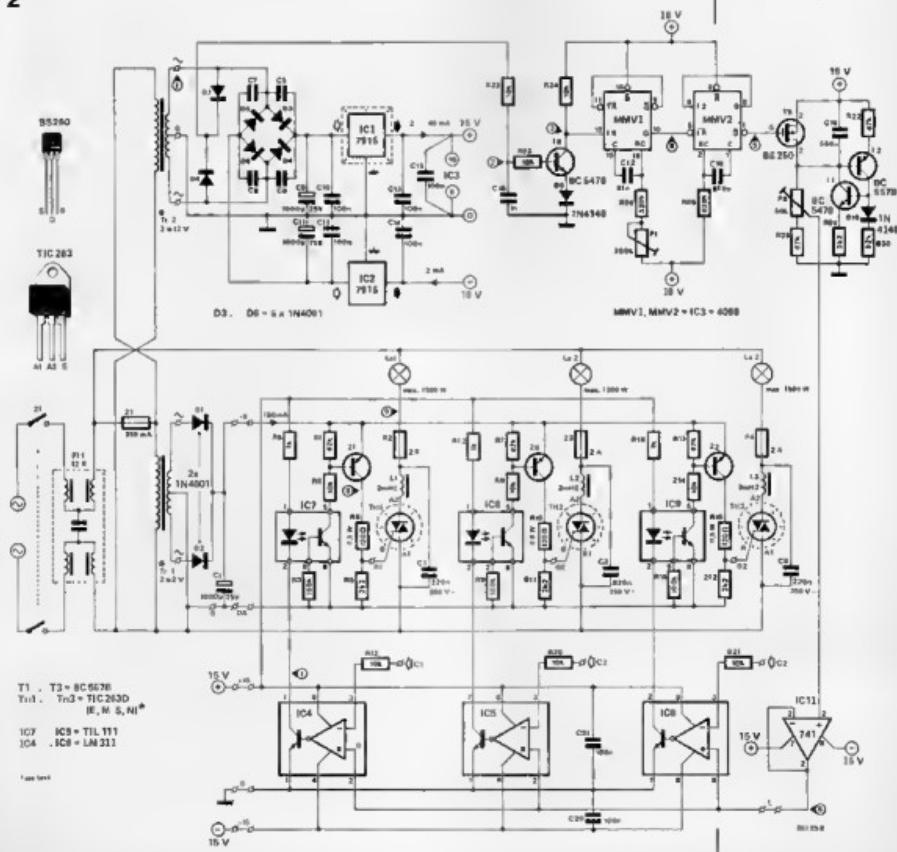
This arrangement gives greater immunity from interference on the mains voltage, and ensures that the pulse output by MMV_1 controls the relevant circuitry precisely

Curve shaping

When the phase gating angle is changed in direct proportion with the slide potentiometer, the brightness of the associated lamp does not change linearly. One of the reasons for this is that the power contained in sinusoidally changing voltages and currents varies not linearly, but according to the

Fig.2 Circuit diagram of the power stages

2



function $f(x) = \sin^2 x$. In addition, there is no linear relation between the power applied to a lamp and its brightness.

The empirical relation between the brightness and the phase gating angle is shown in Fig.4. The peculiar shape of this curve is also found in Fig.3 (6).

The circuit around T_5 , T_6 , and T_7 serves to delay the gating in such a way that the relation between the voltages at inputs C_1 , C_2 , and C_3 and the brightness of the associated lamps is linear. This happens as follows: At each pulse generated by MMV_2 , T_5 conducts and short-circuits C_{19} . The potential at the junction of P_2 and C_{19} is then +15 V. At precisely the moment the mains passes through zero, the pulse from MMV_2 ceases. T_5 switches off immediately and C_{19} begins to charge via P_2 and R_{25} : the potential

across P_2 drops. As soon as the voltage across C_{19} reaches the 0.6 V threshold of the base-emitter junction of T_6 , the capacitor is charged more rapidly by the current through T_6 , T_7 , and R_{25} . The potential across C_{19} continues to rise, while that across P_2 drops. When the voltage across P_2 has fallen to 1 V, the current through T_7 has become very small, and the voltage drop begins to slow down. The entire process, with component values as shown, lasts about 10 ms. After that period, a new pulse from MMV_2 starts a fresh discharge-charge cycle. The resulting "bent" sawtooth signal is buffered by IC_{10} , and then used by comparators $\text{fC}_4 \dots \text{fC}_6$ as a reference voltage.

Fig.3 Timing diagram of the power stages

3

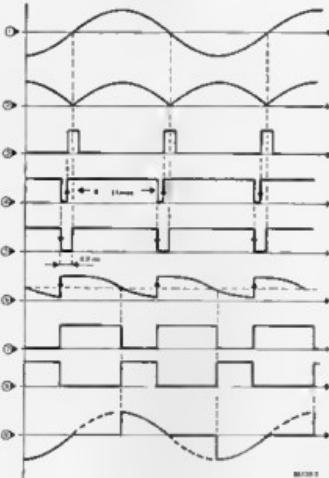
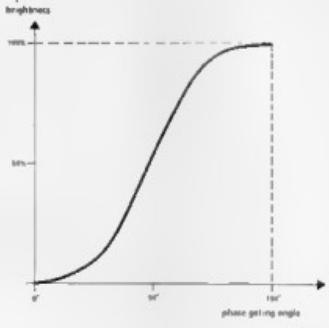


Fig.4 Lamp brightness vs phase gating angle characteristic

4



Phase gating

$\text{IC}_4 \dots \text{IC}_6$ compare the input voltages at C_1 , C_2 , and C_3 with that provided by IC_{10} — Fig.3 (6). If the latter is larger than the input voltage, the outputs of the comparators are logic 1 and the LEDs in the opto-isolators remain out. If the situation at the comparators were reversed, their outputs would be 0, and the LEDs would light. Fig.3 (7) shows the output level of the comparators when the potential at the C inputs is 6 V. This corresponds to the slide potentiometers set at exactly the centre of their travel, and results — in this case — to a duty factor of 50 per cent. These logic levels are inverted by the transistors in the opto-isolators and then fed to transistors T_1 , T_2 , and T_3 . The resulting pulses at the gates of the triacs are shown in Fig.3 (8). The curve in Fig.3 (9) shows that phase gating takes place during alternate half cycles of the mains voltage.

Construction

The power stages have been divided over two printed-circuit boards: Fig.5 shows that for mains unit ff, the zero crossing detector, and the curve shaper, incl. IC_{10} , while that in Fig.6 contains the comparators, optoisolators, and trigger circuits for the triacs. The triacs themselves are fitted on small boards that are cut off the board in Fig.6 along the dotted lines. Connecting wires should be stranded with a diameter of not less than 1.5 mm. It is essential that the power sockets and mains switch are rated at 240 V, 15 A, in the 3600 W (3-channel) version — see Fig.8.

It is, of course, possible to use other configurations than that in Fig.8. For instance, Fig.9 shows a rather larger unit with nine channels (three per mains phase) each of 1200 W rating, for operation from a three-phase mains supply. This version must, of course, be fitted with a suitably rated, three-way mains switch.

Another configuration is to build the version of Fig.8 twice and connect the two in parallel to the normal single-phase mains supply. Provided they are cooled adequately, Type TIC226 triacs may be used, and these should be protected by 6 A fuses. Otherwise it is advisable to use Type TIC263 devices: these have the advantage of being

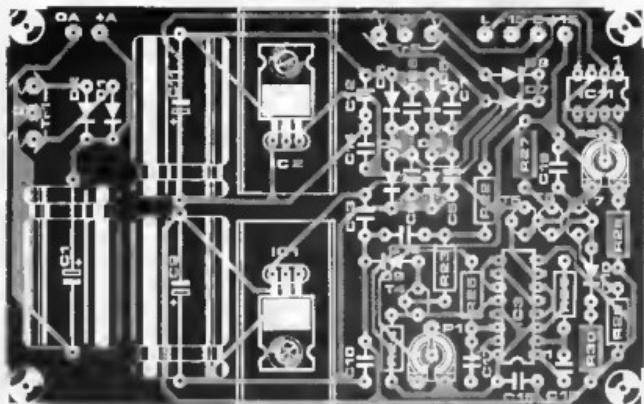


Fig.5 PCB for mains unit II, zero crossing detector, and curve shaper (incl. IC1).

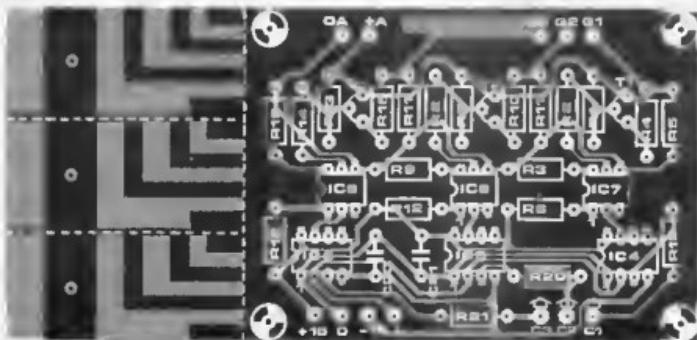


Fig.6 PCB for the comparators, opto isolators, and triac trigger circuits. The track sides of these boards are given on pages 42 & 43.

Fig.7 Wiring of a triac



Parts list

Resistors

R₁, R₇, R₁₃, R₂₇, R₂₈ = 47 k
 R₂, R₈, R₁₄, R₁₉ = R₂₄ = 10 k
 R₃, R₉, R₁₅ = 100 k
 R₄, R₁₀, R₁₆ = 120 Ω, ½ W
 R₅, R₁₁, R₁₂, R₂₉ = 2k2
 R₆, R₁₂, R₁₈ = 1 k
 R₂₅ = 330 k
 R₂₆ = 820 k
 R₃₀ = 82 k
 P₁ = 250 k preset
 P₂ = 50 k preset

Capacitors

C₁ = 1000 μF, 16 V
 C₂ = C₄ = 220 n, 630 V
 for 240 V AC!
 C₅ = C₆ = 22 n
 C₉, C₁₁ = 1000 μF, 25 V
 C₁₀, C₁₂ = C₁₅, C₂₀^{*}
 C₂₁ = 100 n
 C₁₆ = 1 n
 C₁₇ = 47 n
 C₁₈ = 470 p
 C₁₉ = 560 n

Semiconductors

T₁ = T₃, T₅ = BC567B
 T₄, T₇ = BC547B
 T₅ = BS250
 IC₁ = 7815
 IC₂ = 7915
 IC₃ = 4098 or 4528
 IC₄ = IC₆ = LM311
 IC₇ = IC₉ = TIL111
 IC₁₀ = 741
 T_{H1}...T_{H4} = TIC226 (D,E,M,N,S)*
 D₁...D₆ = IN4001
 D₇...D₁₀ = IN4148

Miscellaneous

means filter, 240 V, 15 A*
 means on/off switch;
 double pole, 15 A
 three heat sinks for triacs,
 8 K/W
 three chokes: 2.2 mH, 5 A
 (TIC226) or 2.2 mH, 7 A
 (TIC263)*
 right angled heat sink for
 IC₁
 three fuse holders for panel
 mounting
 three fuses: 6 A (TIC226) or
 8 A (TIC263)*
 T_{R1} = 2 × 6 V, 0.2 A
 T_{R2} = 2 × 15 V, 0.1 A

* see text

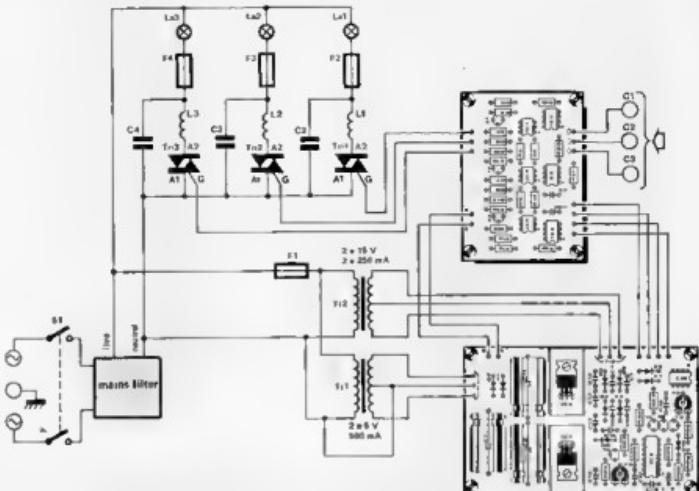


Fig.8 Wiring diagram of the simplest version with three channels, each rated at 1.2 kW

able to withstand the surge when a 1000 W or 1200 W lamp burns out. These types should definitely be used when the configuration of Fig.9 is used with only two channels per mains phase i.e., six channels with a power handling of 1800 W per channel.

If three boards as shown in Fig 6 are used, and each is fitted with only one comparator, one opto-isolator, and one triac, a three-phase installation with three channels — each rated at 3300 W — is obtained. The TIC263 triacs must then be protected by 15 A fuses. Suitable chokes for this version

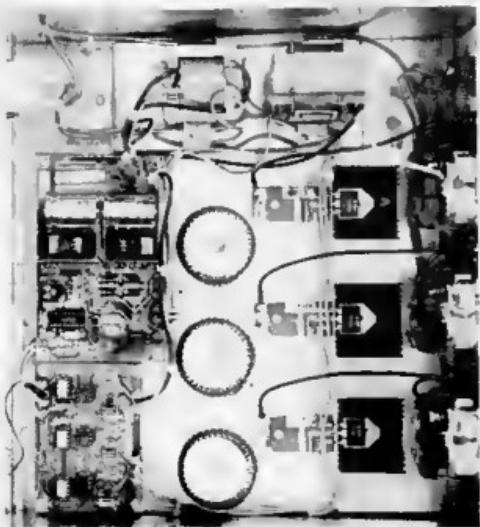
will be difficult to obtain; it is best to make them yourself. They should be wound like a coil in a loudspeaker cross-over network with enamelled copper wire of not less than 2 mm² cross-sectional area.

Setting up

Before any setting up is attempted, carefully check all wiring, because on the one hand, mains voltages are present at several places in the circuit, and on the other, some of the components are not cheap. Once you are sure everything is in order, connect the mains to the power stages and check with a multimeter (not digital) set to the 300 V AC range whether there is AC present between the three C-inputs and the — earthed! — enclosure. If the meter indicates 240 V, there is a fault in the wiring or T_{r1} is defect; if it shows between 0 and 30 V, everything is all right. Such a small voltage is normally caused by random quiescent currents, which require no further attention.

Connect the outputs of the control panel to the inputs of the power stages by a suitable cable. Load each channel with a flood light, spot light, or whatever other lamp may be required.

Adjust the controls for each channel in such a way that the relevant lamp just lights. Next, adjust P_1 in the power unit so that the lamp(s) flickers in a regular rhythm. Then adjust P_2 so that the lamp(s) just cease to flicker: this is the correct setting for P_1 . Finally, adjust the control panel for maximum brightness of the lamp(s); adjust P_2 in the power unit initially so that the lamp(s) begins to dim, and then turn this preset in the opposite direction until the brightness no longer increases.



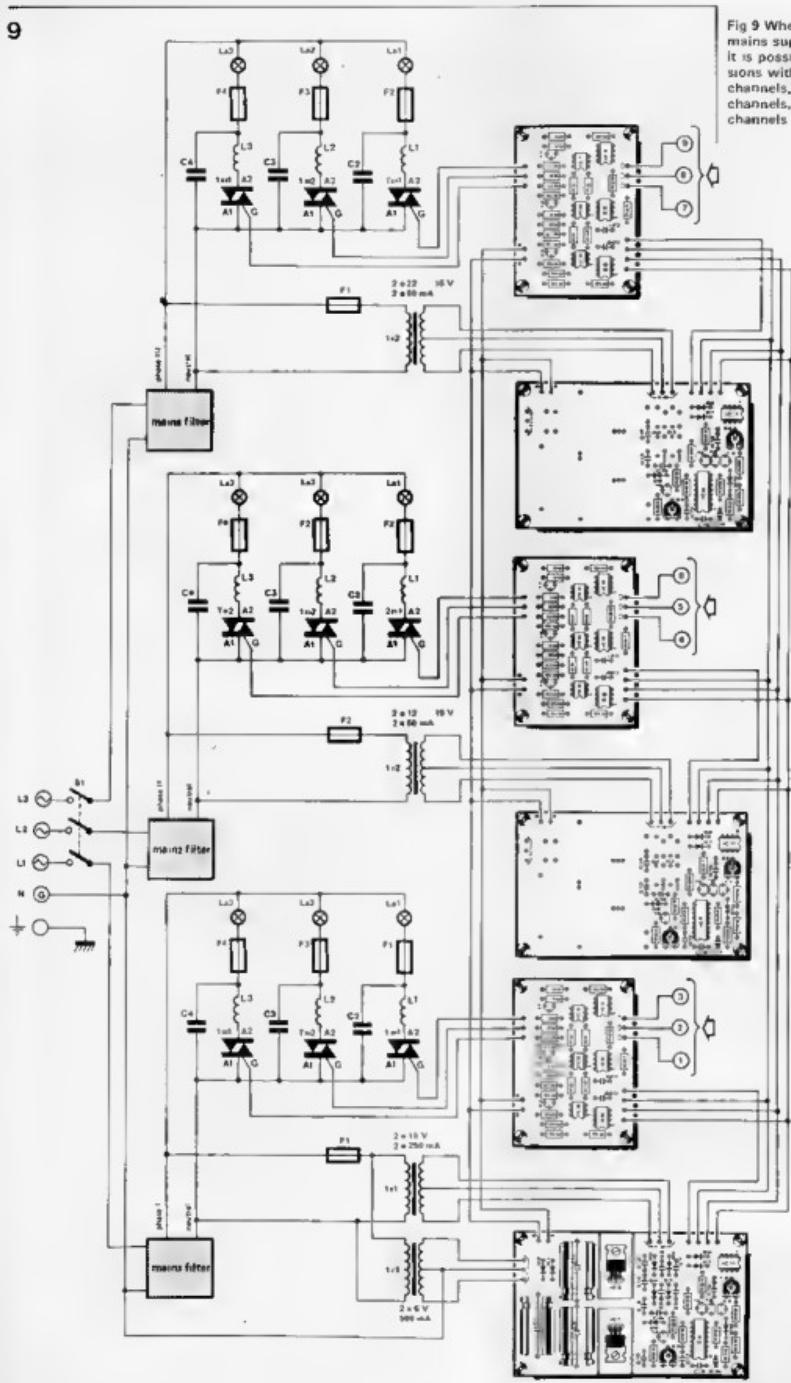


Fig 9 Where a three phase mains supply is available, it is possible to use versions with nine 1200 W channels, six 1800 W channels, or three 3600 W channels

Artificial intelligence: a myth or a moneymaker?

by Professor W B Heginbotham, DSc

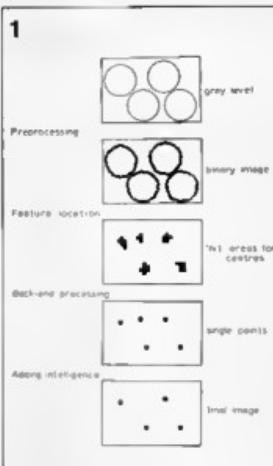
The term artificial intelligence (AI) means different things to different people. Its interpretation largely depends on the background interests of the individual, but if one takes an unbiased viewpoint categories can still be established.

The first activity area can be identified by the notion that in some way computers can be made to duplicate the human intellect. Their use for evaluating highly complex theories in physics, chemistry, and cosmology is in no way unusual these days, perhaps computer based studies to evaluate theories of neurophysiology and psychological phenomena will eventually lead to a better understanding of the human central nervous system. It is interesting to speculate what progress the alchemists of old would have made with the assistance of modern computing methods. After all, the practical benefit of alchemy was a spin off from its main theme with the inadvertent establishment of the basis of modern chemical science. A similar by-product could be derived from any attempt to create synthetic humanoid responses.

The main restriction in the development of practical AI until now has lain in the vast amounts of computing required, with the consequent high costs and slow responses. This has led to a disappointing level of ability to solve real everyday problems, particularly those of industrial production, both on the shop floor and in functions such as production control. With the development of very large scale integrated (VLSI) systems, however, these restrictions will be significantly reduced in future.

Designs Outstrip Reality

For instance, the number of interconnected paths that can theoretically be concentrated on one chip can only be visualized by making an analogy with the entire street systems of the two American states of California and Nevada. Chip design techniques have outstripped practical capacities to actually generate this number of interconnections. Maybe AI will beget more AI as the method is set to work to solve its own physical problems. Future applications will be profoundly influenced by the development of expert systems, sometimes referred to as knowledge based systems. The idea behind these is to enshrine the



Stages of processing in the BRSL imaging system.

experience of a human operator as a set of rules so there is no need to work everything out from scratch. Theoretically, this reduces the problem to more manageable dimensions, but as yet such methods are in their infancy and can handle only around 500 to 1000 facts. There are less than ten such systems currently working in practice worldwide and the majority are concerned with medical diagnostics. To apply AI successfully and economically, it is necessary to identify areas of

activity that fit the technology available. The use of artificial vision remains the most active area of application.

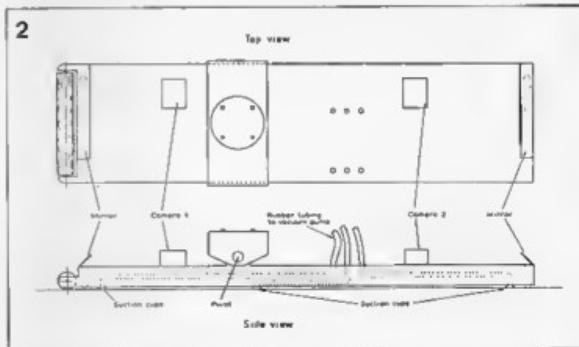
Bin Picking Problem

The United Kingdom is one country that has never lagged behind in research into the concept of artificial vision and the amount of effort being put into this activity by universities, research organisations — both government sponsored and independent — and private industry is quite significant. This is illustrated by the following account.

In-process handling and machine feeding still cause difficulties, particularly for variable batch production and semi-ordered production. There have been numerous attempts by researchers worldwide to solve the bin picking problem so as to enable machines to select individual components from parts stored loosely in bins or containers, so imitating human action.

However, the fully generalized three dimensional bin picking problem has far too many degrees of freedom for economic solutions to be applied at this time. Therefore, **stack picking**, where the parts are not completely randomly positioned but are in a partially ordered state, is a much more practicable situation.

British Robotic Systems Ltd (BRSL) has implemented practical stack picking for loading/unloading a flexible manufacturing system (FMS) turning cell. Initial investigation to prove the system was carried out with a BRSL Autoview Viking system. The vision



Gripper for handling flexible composite materials.

processing algorithm consists of several stages — preprocessing, feature location, back end processing, adding intelligence, and final checking.

A Matter of Processing

It has been found sufficient to use a 128×128 pixel matrix for viewing the components. The preprocessing stage takes in a set of grey level images and reduces them to a binary image suitable for next stage processing. A high-pass filter is applied to the original image of the parts to improve feature extraction. By this means, much of the noise is removed from the image scene, concentrating analytical effort on to essential information processing.

Feature extraction uses simple diameter measurement, which, when found to be within known limits, identifies the component. The back end processing determines the centres of the parts within a cluster for a single layer and records successes as hits. Positional determination accurate to ± 17 mm for a 1 m square bin stack can be achieved. By the use of an extra module, estimates of the centre of the area of parts can be improved to ± 4 mm if required. This latter figure is sufficient to enable a robot mounted gripper to retrieve a component.

Another example of the application of AI can be found in the vision guided cutting machine developed by Westland Helicopters' advanced manufacturing development department. Sheet metal components were the subject of this development, whereby computer numerical control (CNC) routing machines cut out flat profiles, but left them as nests within the parent sheet until a later stage. This facilitated easy in-process handling to the degreasing and deburring operations.

Removing Tags

Parts were finally separated by a detagging operation. Artificial intelligence, in the form of machine vision, was used to control an automated detagging machine so that accurate separation of components from the flimsy and sometimes distorted parent sheet was achieved. The vision system used a DEC11/23 computer and was interfaced to a Siemens CNC machine controller.

Vision transducing was by 384×576 picture element cameras, supplied by BRSL and arranged to view the tag area through an Olympus Borescope. Illumination of the viewed areas was by a 10 mm fibre optic light guidance system fed from a 150 W bulb. By angling the light source appropriately, well defined sharp edges were created so as to aid reliability of image transducing.

Tags, approximately 3 mm wide, varied according to the size of the cutting tool used. It was necessary to remove tags without running below the edge of the general line of the component and not to leave a protrusion of more than 0.1778 mm. Tag cutting was carried out by a slitting saw system.

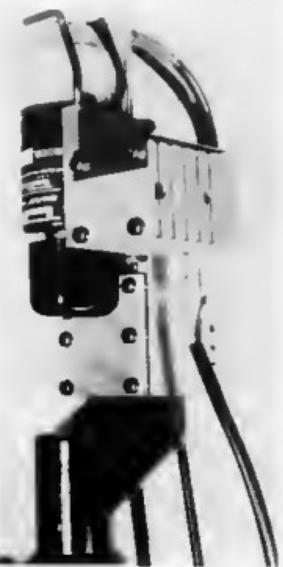
Other practical applications of artificial intelligence are found in process control activities, and this theme will be continuously expanded as and when appropriate processes are capable of being understood and represented accurately by computation.

High Intensity Energy Beam

A good example of an appropriate process is plasma welding, and the following is a typical example of a British university industrial project. This is aimed at investigating the possibilities for AI controlled plasma welding with integral arc guidance and is being carried out at Coventry (Lanchester) Polytechnic.

Plasma is a high temperature region of ionized gas stimulated by an electric arc, which can be focused to form a high intensity energy beam. Because of this feature, the process is much less sensitive to variations in arc length than the gas tungsten arc system.

The experimental system was based on a Unimation PUMA robot, connected to a British Oxygen Company Sabre arc micro plasma unit with a maximum current output of 15 A. By the application of a magnetic field, an electric arc can be deflected. The direction or arc movement is dependent



The electromagnetic arc deflector fitted to a plasma welding torch.

on the polarity of the magnetic field and the arc polarity. This provides a system of weld control that has virtually no lateral inertia. Essential processes normally carried out by human beings, such as weaving, can therefore be carried out very effectively by a programmed variation in magnetic field intensity and polarity. Superimposed sinusoidal arc weaving at 2 Hz can improve weld conditions quite significantly.

Great Potential

This concept is laying the foundation for a highly interactive welding system capable of being controlled by AI to produce high quality welds automatically. The relative ease of welding arc direction control will also assist in automatic seam tracking to follow weld lines that are not well determined.

This feature will improve the prospect of achieving small batch weld automation by reducing dependence on expensive welding jigs. The system also has great potential because it can be applied successfully to the welding of materials like aluminium, which cause difficulties even for human manipulative intelligence.

The handling of non-rigid sheets of compliant material poses a problem for automated handling. Assembly of aerospace structures from composites requiring lay-up of carbon fibre profiles is a major problem.

The University of Hull has developed a sensory gripper that provides visual feedback from two gripper mounted linear array cameras, permitting accurate alignment and lay-up of carbon fibre composites. It has always been the hope that artificial intelligence would provide the key to automation of the production of structural composites. While it is possible to rapidly program a robot arm with a movement sequence to deal with small batches of structural composites, the actual act of laying-up poses severe mechanical problems in terms of how one transports and positions compliant materials.

Visual Sensing

The gripper especially designed for this has six suction cups on the underside face. These are connected through rubber tubing to a vacuum pump to provide the means of supporting pre-cut profiles. To cater for the case when all vacuum cups are not in contact with the material, this gripper can operate five cups open to the atmosphere while the single remaining one holds on to a flat surface. Visual sensing is provided to monitor profile position and ensure a quantitative check on the final jointing of lay-up sheets. This is achieved by two 256 element charge couple device

(CCD) linear array cameras, mounted on opposite ends of the gripper. The available resolution of this system is ten pixels per millimetre, considered adequate for the application under consideration.

A single line of pixels provides all the necessary information to determine edge position of the profile. A mirror is used in conjunction with each camera to allow two slits, each 25 mm wide, to be viewed by high power light emitting diodes. The gripper is used mounted on the arm of a PUMA robot and addresses pre-cut composite profiles that are pre-stacked but have some positional variation.

This is a prototype development but illustrates the problems of applying AI to deal with problems of variability at the workplace.

Knowledge Based System

The University of Edinburgh is particularly active in developing robot programming languages, and notably the robot assembly programming technique (RAPT) system. This is knowledge based and an illustration of the

power of combining knowledge bases with artificial intelligence.

The RAPT modelling system is an object level robot programming arrangement in which the parts to be handled and the robot work station are described in terms of their surface features. These can be plain or spherical faces, cylindrical shafts or holes. Straight edges and vertices are represented as very small diameter cylindrical and spherical features respectively.

An assembly program is defined in terms of a sequence of distinct requirements defined by the programmer to meet a progression of workplace needs. Therefore, the RAPT system provides for planned assembly relationships for components and monitors the difference between planned and actual positions by applying machine vision.

This is done by:

- Specifying which features of a particular object are to be sought, with which camera. This is the look command.
- Describing in broad terms the maximum uncertainty expected in the

position of an object being viewed. This is the tolerance command.

- Specifying limitations on uncertainties in terms of spatial relationships. This is the inviolate command.

Languages Enhanced

By using this combination of RAPT and visual verification, it has been shown how vision can be used to enhance object level robot programming languages. By the addition of such a knowledge based solid modelling system, a powerful programming aid is created because no assumption about positions of cameras or about the manner of presentation of objects to the vision systems is required. This information is naturally included in the object level program as it is written.

(LPS)

Capacitors and resistors: some recent developments

by H A Cole, CEng, MIEE

Despite the ever growing influence of integrated circuit technology, demand for the ubiquitous resistor and capacitor shows no signs of fading. In the United Kingdom, for example, the capacitor market last year was worth in the region of £130 million, and is expected to grow substantially in 1985. A little more than 10 per cent of this was accounted for by the tantalum capacitor, which is likely to be in increasing demand in the next few years — especially in chip form for surface mounting assemblies.

Tantalum is a material with many remarkable properties as far as capacitor manufacture is concerned. Unfortunately, it is also very expensive. An interesting statistic that illustrates the capacitor's importance is that more than half the tantalum mined is used in the manufacture of such devices.

Production of tantalum capacitors in Britain, and recently in much of Europe, is dominated by STC. This has come about as a result of STC's acquisition in 1983 of the tantalum capacitor operations of SEL at Bislohe, in West Germany, and of Union Carbide at Aycliffe. With these two plants complementing its existing tantalum facilities at Paignton, Devon, STC

hopes to capture a substantial slice of the world market for tantalum capacitors, which in 1984 stood at about £50 million, with almost half in the United States of America.

Expanded Production

STC also believes it is now in a much better position to build up its present share of the £45 million world market for surface mounted chip devices, and to expand its production of dipped, metal case, and moulded tantalums. Representative of the wide range of tantalum capacitors from STC are the TAP and TAG series. These are resin dipped, radial lead types approved to IECQ 300-201-GB0001 and BS CECC 30-201-027. The capacitance range extends from 0.1 to 680 μF at operating voltages of 3 to 50 V.

The TAA series features hermetically sealed, axial lead types with additional approval to MIL-C-39003. Their capacitance range runs from 0.1 to 330 μF at operating voltages of 6.3 to 63 V. Then there is the TAQ series of chip-type tantalums in seven different sizes, all suitable for direct bonding and auto-insertion. These have a capacitance range of 0.47 to 100 μF at

operating voltages of 6.3 to 35 V. A particularly interesting type of tantalum from STC is the CA series. These are etched foil capacitors in a hermetically sealed silver case and approved to DEF 5134. They are available in both polar and non polar form with axial leads, and have a capacitance range extending from 0.68 to 1500 μF . Operating voltage runs from 6 to 160 V.

Coupling, Filtering, Suppression

The ceramic based capacitor is one of the oldest and most reliable types, and is still widely used for such applications as coupling, filtering, suppression of radio frequency interference, and the protection of sensitive semiconductor devices. The United Kingdom market for ceramic capacitors was worth more than £30 million in 1984, and a substantial proportion was supplied by STC from its two manufacturing plants in eastern England. Its Norwich plant is a totally integrated facility devoted entirely to the manufacture of multi-layer ceramic capacitors. It undertakes the entire operation, from the development of raw materials to the shipment of fin-

ished products.

An interesting example of ceramic capacitor technology is the FLT radio frequency interference filter manufactured by Oxley Developments. The filter is in effect a π -section assembly of two ceramic tubular capacitors interconnected by a special ferrite material that ensures good insertion loss figures at load currents of up to 10 A. The filters are available in two case styles and with two capacitance values. One case has an M5 fixing thread, while the other has a 12UNEF thread. Minimum capacitance values are either 1500 or 5000 pF, giving minimum insertion loss figures of 45 and 50 dB respectively over the frequency range 200 MHz to 1GHz. The working voltage is 350 V dc for both capacitor types over an operating temperature range of -55°C to 85°C . Oxley Developments also manufactures an impressive range of ceramic discoidal lead through and tubular chassis mounting, high voltage, filter capacitors, ranging in value from 22 to 10 000 pF at working voltages of 50 to 500 V dc. All are manufactured in Britain according to BS5900 and DEF-STAN 05 21 requirements.

The manufacture of mica capacitors began in Britain more than 60 years ago. Although the original manufacturing technique of using alternate layers of mica and tinned copper foil has long since been replaced by the silvered mica method, the mica capacitor is still in great demand for applications demanding exceptional reliability.

Low Power Factor

Apart from their outstanding reliability, mica capacitors are physically rugged and exhibit excellent performance at high frequencies and in pulse applications. They also have a very low power factor and close tolerance of capacitance. Typical applications include oscillators, logic and transmission circuits, and pulse forming networks. A particularly valuable property of the mica capacitor, which has been of importance only since the introduction of nuclear power, space flight and guided missiles, is its relative insensitivity to radiation originating from nuclear reactors and outer space. STC manufactures an impressive range of silvered mica capacitors, as does MPE-Dubilier. The STC capacitors range in value from 4 to 100 000 pF, at voltage ratings of up to 400 V and in various case styles. MPE-Dubilier makes a specialized range of capacitors suitable for smoothing 12 kV, 70 kHz power supplies delivering 22 A continuously, and for use in pulse forming networks operated at up to 21 kV.

The United Kingdom resistor market for 1984 was worth about £65 million and is not expected to increase very

much this year. This is because manufacturers are now able to design out discrete resistors, which means fewer are required for new products. A good example of this is in the domestic colour television receiver. In 1981 it would have contained more than 200 discrete resistors, while today the same type of receiver has fewer than 150.

On the other hand, the impressive improvements made in resistor manufacturing technology during the past decade or so mean that very high quality resistors are available to designers at prices that make them competitive with traditionally cheaper alternatives with much inferior performance. This applies particularly to the metal film types, which are largely replacing the moulded carbon and carbon film resistors and are being used increasingly for surface mounting application. This says much for the advances made in manufacturing technology when it is remembered that the metal film resistor has been around for at least 30 years.

Competitively Priced

Conductive plastics have been available for more than 20 years, but it

is only in the past five years or so that the technology has developed to the stage where such materials can be used for the manufacture of competitively priced potentiometers.

The basic constituents of a conductive plastics potentiometer track are carbon and resins, together with modifying agents that ease the processing and improve the performance. Conductive plastics tracks enable manufacturers to produce inexpensive, long life potentiometers featuring high accuracy, low wear, low operating torque, and high resolution. Another advantage is that tracks can be produced to virtually any shape of resistance law.

Representative of the latest technology in this field is the 11SB potentiometer manufactured by Ferranti. In fact, this particular potentiometer is available both as a conductive plastics and a wire wound component, and if necessary multi-gang versions can be constructed using a mixture of the two types. The 11SB is used extensively in applications where the height from the mounting surface is critical.

(LPSI)



A selection of the many types of capacitors manufactured in Britain by STC



audio sweep generator

This sweep generator is intended primarily for use with the Function Generator described in the January 1985 issue of *Elektor Electronics*, but can also be used with other types. It varies the output frequency over a predetermined range of values so that the two units together can be used to investigate the behaviour and frequency response of, for instance, an electronic filter or amplifier.

by P Theunissen

When the sweep generator is used with a function generator other than that described in the January 1985 issue of *Elektor Electronics*, it should be noted that the VCO <voltage-controlled oscillator> must be capable of operation over an input voltage range of 0.1 V to 10 V, corresponding to a frequency ratio of 1:100. If not, a suitable level adapter should be used.

Block schematic

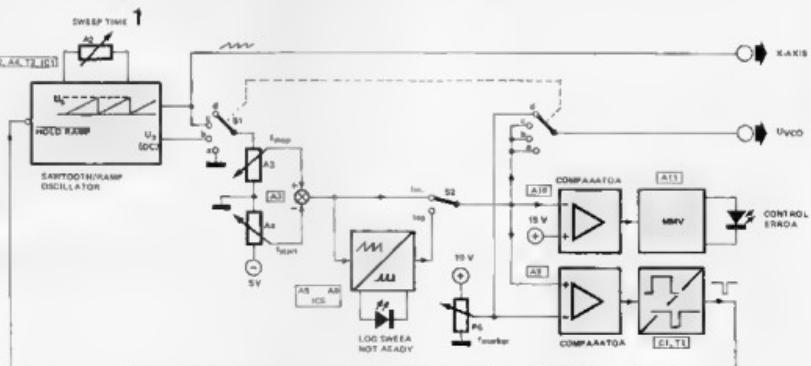
The generator provides the signals that are necessary to display, for instance, the frequency response of a filter on an oscilloscope. The fundamental requirement of a sweep generator is a sawtooth or ramp oscillator. Since the oscilloscope during wobulating operates in the *xy* mode, its internal horizontal time base must be dis-

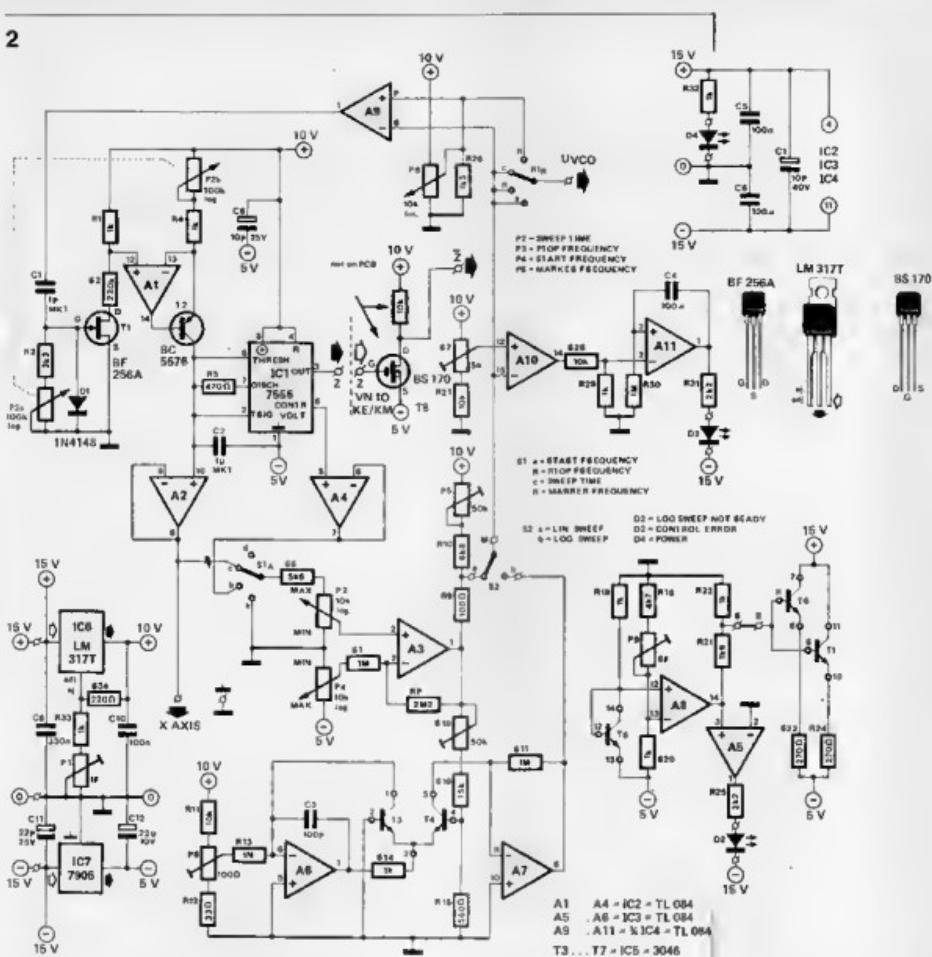
abled and replaced by an external one. This external sawtooth oscillator also drives the VCO in the function generator. When the sawtooth signal is zero, the VCO frequency is low, and the electron beam is at the left of the screen. When the level of the sawtooth signal rises, the VCO frequency increases, and the electron beam is deflected to the right. In this way, the (horizontal) *x*-axis is produced on the screen.

The vertically varying quantity is displayed by the vertical time base (*y*-axis). If, for instance, the output of the function generator is applied to the input of a filter, and the output of the filter to the *y*-input of the oscilloscope, the screen will display the frequency vs voltage response of the filter.

The period of the sawtooth generator in Fig.1 may be varied between 100 ms and

Fig.1 Block schematic of the sweep generator.





10 s, so that even for low frequencies a sufficiently long-duration sawtooth is available. Before the sawtooth signal is applied to the VCO input of the function generator, its stop and start frequencies are preset by P_3 and P_4 , respectively. Changing the zero level of the sawtooth with P_4 affects the minimum VCO voltage and, therefore, the minimum frequency. Preset P_3 alters the peak value of the sawtooth, which determines the maximum VCO level and, consequently, the upper frequency limit. The frequency limits are easily preset with the aid of a frequency meter. An erroneous setting is indicated by an LED.

With S_1 in position a, P_3 is short-circuited, and the sawtooth signal is switched off. A direct voltage, U_{VCO} corresponding to the lowest required frequency, i.e., start frequency, is then set with P_4 . The start frequency may be read from a frequency meter connected to the SYNC OUTPUT

socket on the function generator. The upper frequency limit is set in a similar way, but with the aid of P_3 and with S_1 in position b. The CONTROL ERROR LED lights when the level at the VCO input is higher than the maximum allowed 10 V.

Moreover, a facility is provided to cause the sawtooth to provide a logarithmic instead of a linear horizontal time base. The difference between the two becomes clear from Photographs 1, 2, and 3. Switch S_2 enables switching between the two modes. It is important to note that the setting of the frequency limits is valid for one of these modes only. Therefore, in practice, the time base mode should be selected before the frequency limits are set.

Preset P₆ serves to set the MARKER FREQUENCY. This is required because, although frequencies between the limits can easily be read on the oscilloscope screen when a linear time base is used, this is not so simple

Fig.2 Circuit diagram of the sweep generator. If the Z output needs to be inverted, T₂ and associated components should be added.

Fig 3 Double-sided printed circuit board for the sweep generator

Parts list

Resistors:

R₁, R₄, R₁₄, R₁₈, R₂₀, R₂₂:
R₂₆, R₃₂; R₃₃ = 1 k
R₂ = 220 k
R₃ = 3k3
R₅ = 470 Ω
R₆ = 5k6
R₇, R₁₃, R₁₇, R₃₀ = 1 M
R₈ = 2M2
R₉ = 100 Ω
R₁₀ = 6k8
R₁₁, R₂₇, R₂₈ = 10 k
R₁₂ = 33 Ω
R₁₅ = 560 Ω
R₁₆ = 15 k
R₁₉ = 4k7
R₂₁ = 1k8
R₂₂, R₂₄ = 270 Ω
R₂₅, R₃₁ = 2k2
R₂₉ = 1k5
R₃₄ = 220 Ω
P₁ = 1 k preset
P₂ = 100 k stereo logarithmic potentiometer
P₃, P₄ = 10 k logarithmic potentiometers
P₅, P₁₀ = 50 k preset
P₆ = 10 k multi-turn potentiometer
P₇, P₉ = 5 k preset
P₈ = 100 Ω preset

Capacitors:

C₁, C₂ = 1 μ MKT (metal foil polythene/tinfoil)
(10 mm max. thick)
C₃ = 100 p
C₄, C₅, C₆, C₁₀ = 100 n
C₇ = 10 μF, 40 V
C₈ = 10 μF, 25 V
C₉ = 330 n
C₁₁ = 22 μF, 25 V
C₁₂ = 22 μF, 10 V

Semiconductors:

D₁ = IN4148
D₂, D₃ = LED; 5 mm; red
D₄ = LED; 5 mm; yellow
T₁ = BF266A
T₂ = BC557B
T₃, T₇ = contained in IC₅
T₈ = BS170 or
VN10KE or VN10KM
(optional - see text)
IC₁ = 7555
IC₂, IC₃, IC₄ = TL 084
IC₅ = 3046
IC₆ = LM317T
IC₇ = 7950

Miscellaneous

S₁ = rotary switch 3 pole 4 position
S₂ = single pole change-over switch
2.5 way DIN sockets for panel mounting
BNC socket for panel mounting (Z-output: optional)
extension spindle for P₆ (optional)
enclosure 205 × 140 × 75 mm,
e.g. Vero 075-01411D
front panel foil 85103-F
PCB 85103*

with a logarithmic time base. In the latter case, it is necessary to produce individual scale divisions with the aid of P₆. This is done by setting P₆ in a manner whereby the direct voltage at its wiper is equal to the VCO voltage. A pulse is then generated which holds the ramp for a short time: this produces a bright vertical line on the screen of the oscilloscope as shown in Photographs 1, 2 and 3. This line indicates the frequency that corresponds with the DC level at the wiper of P₆. With S₁ in position d, the marker frequency may be read from the frequency meter. The marker frequency is, of course, also produced with a linear time base.

Note that no sweeping takes place with S₁ in positions a, b, and c!

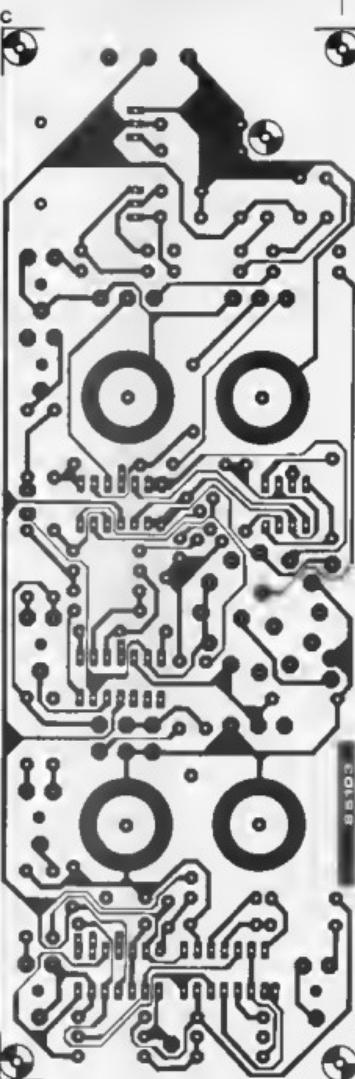
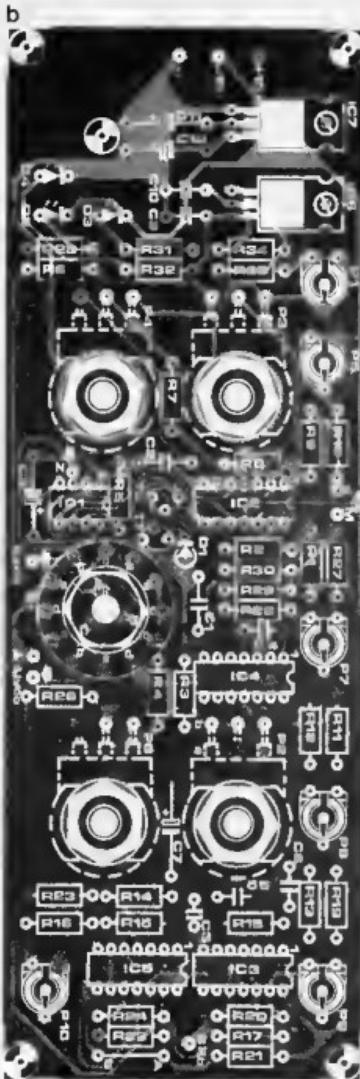
Circuit description

The sawtooth/ramp oscillator consists of A₁, A₂, A₄, T₂, and IC₁ - see Fig 2. Opamp A₁ and T₂ form a voltage-controlled current source that charges capacitor C₂ with a current of 0.45...45 μA, depending on the setting of potentiometer P_{2b}. Timer IC₁ has been connected in such a way that when the voltage between pins 2 and 6 has reached a level of 5 V, C₂ discharges. When the potential across pins 2 and 6 has fallen to 0 V, a new charge-discharge cycle commences. The sawtooth signal is applied to frequency limit setting potentiometers P₃ and P₄ via buffer A₂. The voltages at the wipers of the presets are combined in A₃; this stage also ensures that under normal conditions the VCO is driven correctly. The minimum drive level for the VCO is set by P₆ to about 100 mV for a linear time base. The signal for the VCO input of the function generator is taken from the wiper of S_{1b}. With this switch in position d, the direct voltage set with P₆ (which determines the marker frequency) is applied to the VCO. Differential amplifier A₉ compares this voltage with the sawtooth signal and, if these levels are the same, switches the output to -15 V. The leading edge of this pulse is shaped by C₁, R₃, P_{2a} and then used to switch on field-effect transistor T₁. This causes the ramp to be sustained for as long as the pulse lasts. To ensure that the pulse duration corresponds to the charging period of C₂, it is preset by P_{2a} in direct proportion with the charging period.

The CONTROL ERROR LED lights when comparator A₁₀ is unbalanced, i.e., when the VCO drive is too high (>10 V). The 10 V level is preset with P₇. When this level is exceeded, the comparator toggles which causes pulse stretcher A₁₁ to switch on D₃. At low sweep frequencies this LED flickers. Because the oscilloscope operates in the x-y mode, the flyback is faintly visible. If the oscilloscope has a Z-input, this small deficiency is easily eliminated by connecting the Z-output of the sweep generator to this input. It may be necessary to invert the output or adapt its level as appropriate. The linear-to-logarithmic converter circuit consists of A₆, A₇, T₃, and T₄. Although this circuit is in principle temperature compensated, the compensation is not sufficient for

3a





the value preset by P_6 , the current through T_8 and T_7 decreases. In this way, a balanced condition is reached in which the dissipation in T_8 and T_7 is of a level that keeps the temperature of the chip within narrow limits.

When IC_5 has attained its correct operating temperature, the LOG SWEEP NOT READY LED goes out. The voltage at the output of A_3 is then between -5 V and 0 V.

Construction

Before work is started on the printed-circuit board of Fig.3, the following preparations

should be made in the function generator. The ± 15 V, earth, and VCO lines should be taken to the sweep generator. The +15 V line is tapped at the cathode of D_7 ; the -15 V from the anode of D_6 ; earth from the central pin of IC_4 ; and VCO from pin c of the VCO input socket; the connection between pins a and c of this socket must be cut. The socket can then still be used as input for an external drive voltage, because if a plug is inserted, the drive from the sweep generator is automatically switched off. The four lines are best terminated in a 5-pin DIN socket that may be fitted in the

The following components should be soldered at both sides of the board: C_{12} ; C_9 ; IC_6 (2x); P_1 ; P_5 ; R_1 ; R_2 ; R_{25} ; R_6 ; R_{27} ; R_{12} ; R_{12} ; P_{10} ; C_5 ; R_{15} ; R_{22} ; C_7 ; T_1 ; C_8 (2x); C_4 ; P_6 ; P_2 ; R_{18} ; P_4 ; solder pin +15 V. A short length of bare equipment wire should be soldered at both sides of the board beside the following positions: pin 4 of IC_2 ; pin 1 of IC_3 ; pin 2 of IC_3 ; pin 4 of IC_3 ; pin 4 of IC_4 ; pin 8 of IC_5 . All soldering pins, except those for connecting the X-AXIS terminal, S_{2a} , S_{2b} , and S_{2d} must be fitted at the track side of the board.

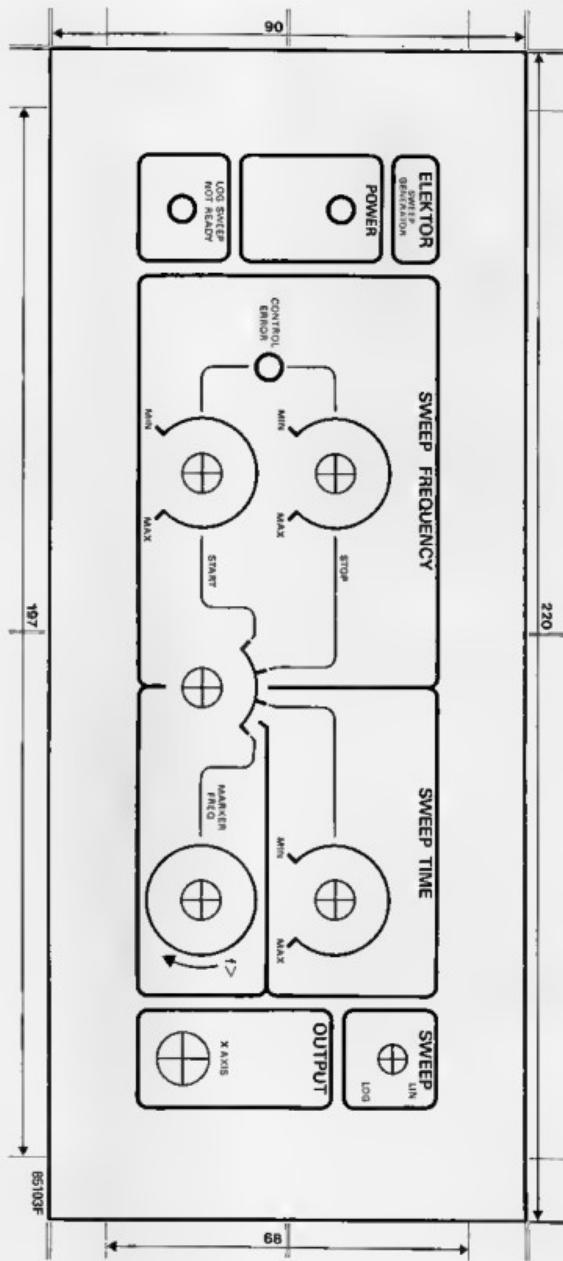


Fig.4 This layout of the front panel foil may be used as a drilling template

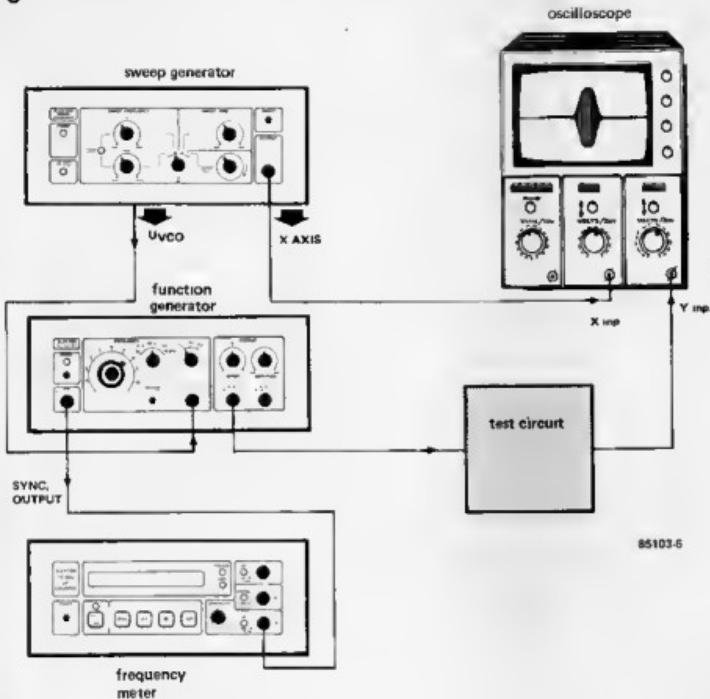


Fig 5 Typical set-up for measuring a frequency response.

rear panel of the function generator. It is also necessary to drill some extra ventilation holes near the 15 V voltage regulator on lid and bottom panel of the function generator to ensure sufficient cooling with the increased dissipation.

The sweep generator may, like the function generator, be housed in a 208 × 140 × 75 mm verobox. Fit a 5-pin DIN socket, similar to that in the function generator, to the rear panel. Where appropriate, also fit a BNC socket for the Z- or Z-output. Finally, remove the two fixing nuts from the lid and bottom panel (these are located roughly where P_9 and P_{10} will be situated).

The corners of the printed-circuit board should be rounded with a file to make them fit snugly into the guides provided in the enclosure.

The front panel should be drilled in accordance with Fig 4. The holes should be properly deburred to ensure that the self-adhesive front panel foil fits smoothly onto the panel. Next, glue the three LEDs into place; fit the SWEEP switch, and then the OUTPUT socket.

Where a mains on/off switch and a second output socket are required, appropriate holes should, of course, be drilled at the same time as the others, otherwise the foil may be damaged!

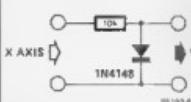
Only when all this preparatory work has

been done should the printed-circuit board be started, but do not yet fit C_1 or link A-B.

Calibration

Once all the connections between the sweep generator and function generator are made, the temperature-compensating circuit must be set. Connect a digital voltmeter between pins 12 and 13 of A_8 and adjust P_9 for a reading of about 60 mV; note that pin 12 is more positive than pin 13. Switch off the mains, and solder wire link A-B on the PCB in place. Switch on the mains again, when after a short time the LOG SWEEP NOT READY LED should go out. Turn P_2 , anticlockwise. Next, connect the XAXIS output of the sweep generator to the Y-INPUT of an oscilloscope as shown in Fig 6. Set the oscilloscope to DC and 50 mV/div. Set the frequency range on the function generator to 1 kHz. Connect a frequency meter to the SYNC output of the function generator. On the sweep generator, set S_1 to position a and S (SWEEP) to LINEar. Turn first P_4 (START) and then P_5 fully anticlockwise. Finally, turn P_4 clockwise until the frequency meter reads 1 kHz. Set S_2 (SWEEP) to LOGarithmic and P_4 (START) fully anticlockwise. Switch off the sweep generator, and turn P_5 fully anticlockwise. Switch on the sweep generator and turn P_5 slowly clockwise until the

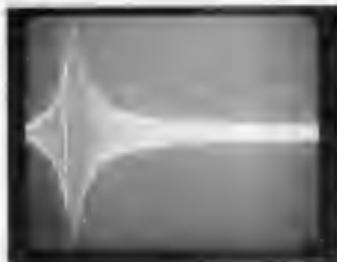
6



Lines= I_{top1} and
logarithmic sawtooth
signals with markers for
frequencies. Scale: 3 V/div.



Sweeping with a linear
time base (24 kHz/div.).



Sweeping with a
logarithmic time base



frequency meter reads exactly 1 kHz. Set S_2 to position b and turn P_4 (START) fully anticlockwise and P_3 fully clockwise. Then adjust P_{10} to obtain a drive voltage, U_{VCO} , of about 11 V.

Finally, turn P_3 (STOP) fully anticlockwise, and set S_2 (SWEEP) to LIN. and S_1 to position b. Turn P_3 (STOP) to obtain a reading on the frequency meter of about 102 kHz, and then adjust P_7 so that the CONTROL ERROR LED just does not light. If the frequency is increased slightly, the LED should light.

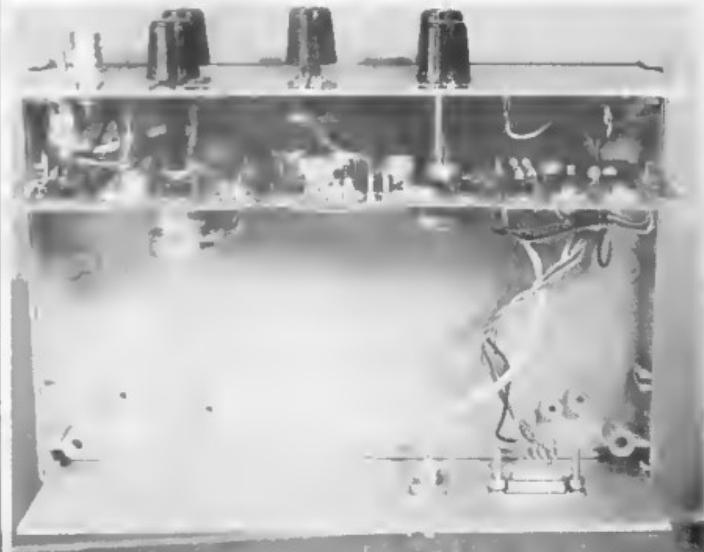
This completes the calibration. Capacitor C_1 can now be soldered in place.

Finally

A typical set-up for measuring a frequency response is shown in Fig.5.

If primarily a logarithmic time base is required, linear types of potentiometer may be used in the P_3 and P_4 positions; this makes setting the frequency somewhat simpler. With the sweep generator connected to it, the function generator should not be operated in the 10 kHz range, because the VCO voltage would tend to drive it up to 1 MHz, whereas its maximum frequency is only 100 kHz.

The photographs give some idea of what the sweep generator can do. A clearly defined frequency response as, for instance, plotted on paper can only be obtained on the screen if the voltage at the Yinput of the oscilloscope is rectified and converted to its logarithmic value. In view of the extra expense, these facilities have, however, not been provided in the present cost-effective sweep generator.



Since this DVM was designed to replace conventional moving coil panel meters, on such things as power supplies, the price was one of the main design considerations. The unit uses only 6 transistors and three CMOS integrated circuits: one IC contains four Schmidt triggers, the other ICs each house a decade counter with built-in BCD-to-seven segment decoder/drivers. It features 2½ digit readout and has an acceptable accuracy.

Basic operation

Conversion of the positive input voltage into a quantity that can be digitally displayed is accomplished by converting the input voltage to a current. This current is then used to control a variable frequency oscillator; the output frequency of this oscillator is a linear function of the input voltage. This frequency is counted by the counter unit and displayed.

The counter unit is controlled by a free running oscillator that determines the gate time for the counter stages and resets them just before the start of each count. It also blanks (turns off) the readout during the brief count cycle.

Circuit operation

At first glance, the input circuit may appear to be confusing, but if one breaks it into smaller units it is much easier to understand.

The heart of the DVM is a current-dependent oscillator. This oscillator consists of the following parts: gate N1, D2, C1 in the charge path and C1, T2 and R2 in the discharge path. The input

MINIVOLT

A.M. Bosschaert

In this age of digital things (?) it is nice to dress up the front panel of home-brew equipment with digital readouts. This handsome little digital voltmeter is easy to build and is inexpensive. In the form presented here, it is a single range unit, intended for use with power supplies

voltage is converted into a discharge current by T1 and T2. These transistors keep the voltage across R2 equal to the input voltage at all times. Since R2 is 1 k, the current through it (the discharge current) in millamps is equal to the input voltage in volts. The discharge time of C1 is therefore a linear function of the input voltage.

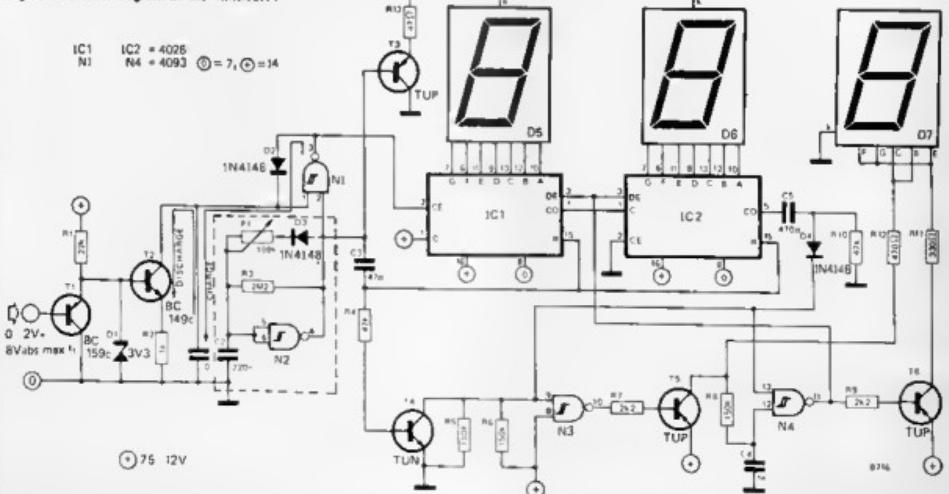
The time required to charge C1 is always the same. The charge current is supplied from the low impedance output of N1.

If for a moment we assume that pin 2 of N1 is held high, the oscillator circuit can be more easily understood.

The secret that allows N1 to operate as an oscillator is the fact that its switching levels are not the same (hysteresis). If C1 is completely discharged pin 1 is low, making pin 3 high. In this state C1 will be charged rapidly. When the voltage on C1 reaches the upper switching threshold of N1, pin 3 goes low. D2 prevents C1 from discharging into the output of N1, and since the input (pin 1) is a very high impedance, the only discharge path for C1 is through

Continued on page No. 12-41

Figure 1. Circuit diagram of the "Minivolt".





fantasia on a MIDI theme

by D Meyer

After God had created man, He rested. After man had created the (analogue) synthesizer, he also rested. But only for a little while, because within a very short time digital techniques had shown a different way, enabling sounds, rhythms, and melodies to be stored in memories. And man realized that he, unlike God, had not created perfection.

The new techniques made the addition of, for instance, digital-to-analogue converters, digitizers, and other peripheral units necessary, so that within a relatively short time the originally simple synthesizer had grown into a complex array of equipment through man's attempts at idealizing it. The magic word was *preset*. And soon the windows of music shops became tangible evidence of a Japanese invasion of relatively inexpensive digital synthesizers. And everybody sensed that music had taken a new lover: the microprocessor.

To make that union a happy one, man hit upon a brilliant idea that would make it possible for communications to be effected between synthesizers, or between a synthesizer and all kinds of modulators, rhythm boxes, mixer units, and many more. And he called it MIDI. Now, a little later, it seems that MIDI is likely to ensure the couple's continued happiness and keep them in perfect harmony.

And so, the device that began with charging and discharging capacitors, oscillators, filters, waveform generators, and keyboards that generate discrete voltages (1 V/octave), is now augmented by all sorts of memory and digital systems that generate and synthesize the most complex sounds. Soon, when digital loudspeakers have become available, there will no longer be any need for digital-to-analogue converters and digitizers, and all that will pass from one unit to another will be 1s and 0s. But since that stage has not quite been reached, some sort of converter is still required, and its operation must be digital. It might be said that as long as a sound is not heard by the listener, it only exists in a purely digital form, i.e., a complex series of digits.

A careful comparison may be drawn between MIDI and the 1 V/octave character-

istic of an analogue synthesizer: both are interface norms. Thus would, however, be a limited one, since MIDI offers many more facilities than this single characteristic. It is, moreover, not so much MIDI itself that offers these facilities, but rather the fact that the music characters are in the form of numbers. And it is well-known that the fast processing systems currently available are more efficient in dealing with numbers, however complex, than with electrical (i.e., analogue) quantities. All the more reason to stress that MIDI is a standard of communication between microprocessor systems that have been designed specifically for music applications.

But MIDI is also an interface that does not contain even a hint of a feature specific to music — see Fig.1 — in the same way that a Centronics interface, often used with printers, has no feature specific to printing. The MIDI interface has no intelligence from a logic point of view; it is nothing but a collection of protocols for data communications and music characters. Therefore, combining MIDI with new electrophonic instruments becomes beneficial only through the richness and diversity of the associated logic programs.

Whether one or a hundred MDIs are added to a monophonic synthesizer, it will not change into a polyphonic one. It is, therefore, the microprocessors attached at either end of the MIDI chain that give the synthesizer a semblance of being intelligent.

MIDI and real time

Ever since the 1950s, there has been an obsession among those engaged on electrophonic music to eradicate the time delays between electronic actions or instructions and their musical result. Such delays, which may vary from seconds to months, are, of course, detrimental. With digital and modern data communication methods, it is possible to reduce such delays to virtually nothing. In music, time is measured in an implacable and rigorous manner, and in a microprocessor with a clock frequency of

several MHz such rigidity is, of course, easily attained. It is possible to transmit and process data and musical characters, prior to producing clear sound signals, so that they appear simultaneous to the listener. This implies that the MIDI interface, via which the data and characters required for the production of a sound are transmitted, does not act as a brake on the general processing. At present, the agreed serial transmission rate is 31.250 kbaud (=31.250 bits/second), which is quite convenient, but already too low for certain sophisticated applications. It is, however, much higher than is tolerated by the majority of RS232 interfaces with which the MIDI may be compared. Additionally, MIDI is typified by perfect decoupling of the different voltages brought about by the interconnecting of a number of different units.

Transmission takes place via an optoisolator, which ensures the absence of earth loops that are often so troublesome in an array of sound reproducing equipment.

The circuit of Fig. 2 offers the facility of using a MIDI in conjunction with an existing RS232 interface, provided the associated microprocessor system is capable of handling the 31.250 kbaud rate. However, this circuit does not provide an external clock to the ACIA that effects the parallel-to-serial conversion. This ACIA may, for instance, be the 6581 on the 6502-based CPU card featured in the November 1983 issue of *Elektor Electronics*. There, the maximum baud rate with a crystal frequency of 1843.2 kHz is 19 kbaud. An external clock may raise this to 125 kbaud. For the present purposes, a crystal frequency of $31.250 \times 16 = 500$ kHz is sufficient. Note that pin 7 of the 6581 should be left unconnected. Once the 31.250 baud rate is established on the existing RS232, all that remains to be done is to ensure that the RS232 levels are passed onto the 5 mA current loop used by MIDI.

Desirable features of the average modern synthesizer

- At least 32 presets to shape the timbre or the registers.
- Touch-sensitive keyboard.
- Single-key modulation with aftertouch. Note that this feature is rarely provided by single key, but is normally common to all keys, although this is not always specified in the manual.
- Variable portamento.
- Pitch bend or modulation wheel.
- 49...88 keys.
- Breath control.
- Transposition.
- Variety of oscillators (voltage-controlled, digital-controlled) and filters (voltage-controlled).
- Envelope generators.
- A number of LFOs (low-frequency oscillators) (it is beyond understanding why even the DX7 contains only one of these circuits).
- Programmable operators and algorithms (it is a major deficiency that the algorithms imposed by the manufac-

1

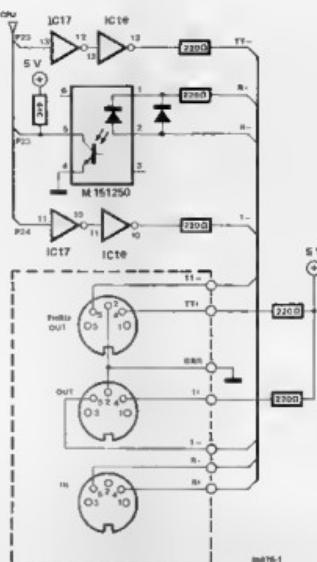


Fig. 1. Schematic diagram of a typical MIDI interface (that of the Yamaha DX7). Note that pin 2 of the Input socket is not connected to earth.

2

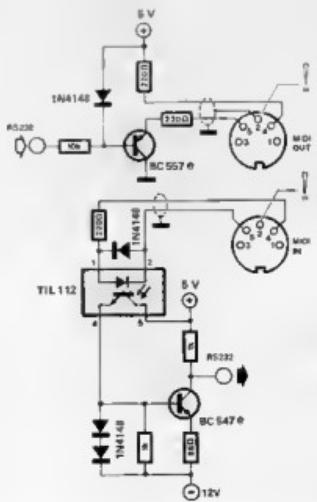
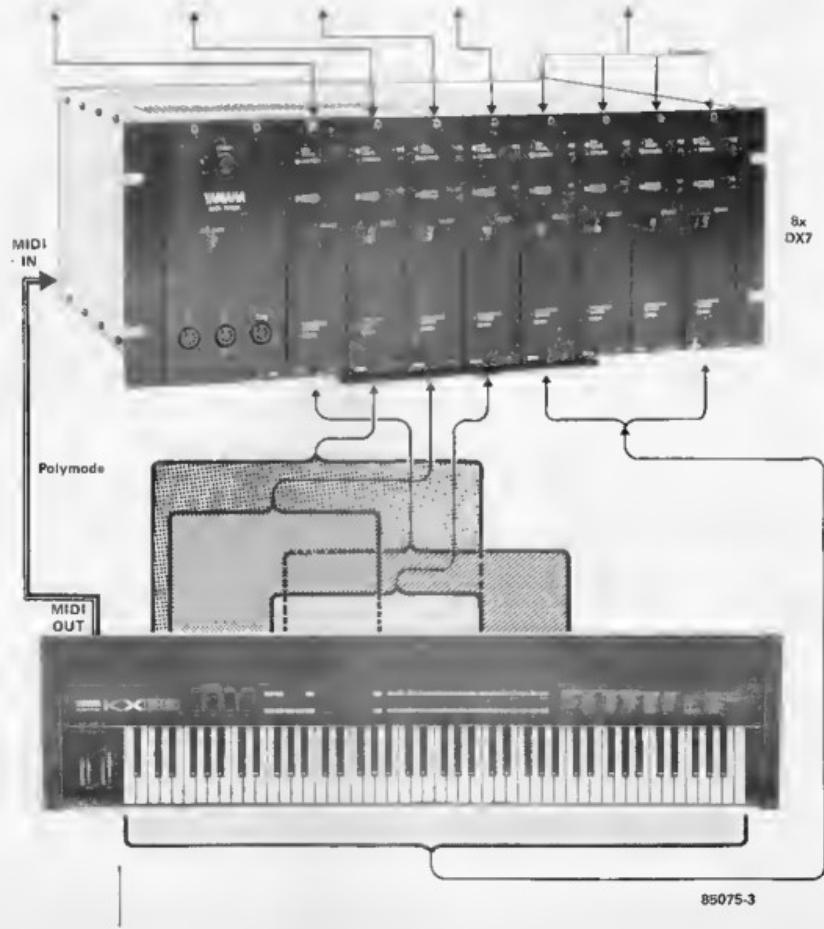


Fig. 2. Wiring diagram of the MIDI interface for use with the RS232 as proposed in this article. This combination enables its use in a chain of communication with any type RS232 interface. Depending on whether negative or positive logic is used, the 0 of the RS232 corresponds to +3 to +25 V respectively.



DX7 → MIDI

TRANSMISSION DATA.

Channel Information

1000nnn Key On & Channel number [n=8, ch1]
 0akkakkk Key number [k=38 C1 - k=88 C8]
 0mmmm Key velocity [m=0, 8, Key OFF]
 [m=1, popl = m=127, HRI]

1011nnn Control change & Channel number
 [n=8, ch1]

0mmmm Control number

0mmmm Control value

C	Parameter	V
1	Modulation wheel	0 - 127
2	Breath controller	0 - 127
4	Foot controller	0 - 127
8	Data entry knob	0 - 127
94	Sustain foot switch	0 - 127
65	Performance foot switch	0 - 127
96	Omni mix = 1	0W min
97	Omni mix = 1	128
98	Omni mix = 1	0W max

1000nnn Program change & Channel number

[n=8, ch1]
 0cccccc Program number [c=0, IR7 (I=8, Ie=31, INT32)
 0p32 CR711 - Ie=63 CR732]

1101nnn Alter voice & channel number
 [ch1]

0mmmm Touch value [0 - 127]

1110mmn Push bender & Channel number [m=0, 1, ch1]

0mmmm Push bender value LS byt [0 - 127]

0mmmm Push bender value MS byt [0 - 64 - 127]

MS byt	LS byt
0 - 84	0
85 - 127	2 (MS byt - 84)

System exclusive information

MIDI active setting

11110000 Status byte

MIDI active setting is continuously output at 80 ms intervals, except during bulk dump data transmission and reverb trim

Bulk data for one voice

11100000 Status byte

01111111 Identification number [I=87 YAMAHA]

0mmmm Soft status [m=0] & Channel number

[ch1]

0f111111 Format number [I=0, 1 voice]

0d0bb0cc Byte count MS byt

0d0bb0cc Byte count LS byt

0d0bb0cc Data 1st byt

0d0bb0cc Data 2nd byt

0d0bb0cc Data 3rd byt

0d0bb0cc Data 4th byt

0d0bb0cc Data 5th byt

0d0bb0cc Data 6th byt

0d0bb0cc Data 7th byt

0d0bb0cc Data 8th byt

0d0bb0cc Data 9th byt

0d0bb0cc Data 10th byt

0d0bb0cc Data 11th byt

0d0bb0cc Data 12th byt

0d0bb0cc Data 13th byt

0d0bb0cc Data 14th byt

0d0bb0cc Data 15th byt

0d0bb0cc Data 16th byt

0d0bb0cc Data 17th byt

0d0bb0cc Data 18th byt

0d0bb0cc Data 19th byt

0d0bb0cc Data 20th byt

0d0bb0cc Data 21st byt

0d0bb0cc Data 22nd byt

0d0bb0cc Data 23rd byt

0d0bb0cc Data 24th byt

0d0bb0cc Data 25th byt

0d0bb0cc Data 26th byt

0d0bb0cc Data 27th byt

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0d0bb0cc Data 31st byt

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0d0bb0cc Data 33rd byt

0d0bb0cc Data 34th byt

0d0bb0cc Data 35th byt

0d0bb0cc Data 36th byt

0d0bb0cc Data 37th byt

0d0bb0cc Data 38th byt

0d0bb0cc Data 39th byt

0d0bb0cc Data 40th byt

0d0bb0cc Data 41st byt

0d0bb0cc Data 42nd byt

0d0bb0cc Data 43rd byt

0d0bb0cc Data 44th byt

0d0bb0cc Data 45th byt

0d0bb0cc Data 46th byt

0d0bb0cc Data 47th byt

0d0bb0cc Data 48th byt

0d0bb0cc Data 49th byt

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0d0bb0cc Data 57th byt

0d0bb0cc Data 58th byt

0d0bb0cc Data 59th byt

0d0bb0cc Data 60th byt

0d0bb0cc Data 61st byt

0d0bb0cc Data 62nd byt

0d0bb0cc Data 63rd byt

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turers do not allow the feedback of several operators superimposed on one another).

- Phase, amplitude, and pulse-width modulation.
- Split keyboard.
- And many more...

This list shows that if all the listed facilities and some others beside are controlled by MIDI, this interface will become very busy, indeed, and yet, there is still no information on the MIDI interface until the synthesizer in question is being programmed with the aid of an external system. This can also be seen from Table I.

It must be understood that all these data are not permanently updated but only when it is necessary to modify one or more of them. But even then, only the data relevant to the characteristic to be altered is transferred. Nothing at all happens about the rest. Moreover, the modification may affect only one of the channels of communication, as it is possible, thanks to MIDI, to serve several individual instruments over the same line, but to address each one separately with data that the others can also understand. An even more restrictive means of communication allows each of the instruments to be addressed separately with specific data that the others cannot understand. These channels allow a microcomputer to control, via the same MIDI interface, not only small and simple synthesizers — polyphonic or monophonic — and smaller units, such as rhythm or other special effects boxes, but also synthesizers that are more complex as far as the number of voices is concerned. It should, perhaps, be stressed again that it is the logic characteristics, and not the channels, that provide the real substance of this system.

Moreover, these channels (at the present time there are sixteen of them available) can be used in three different modes, called OMNI, POLY, and MONO. Briefly, all data available in OMNI are transmitted over all MfDf channels: it is then as if there were only one common channel. In POLY, all data are transmitted over one predetermined channel in such a way that only receivers associated with the channel can receive the data. Finally, in MONO only specific data are transmitted over certain channels. In other words, in the POLY mode it is possible to imagine a trumpet, a saxophone, and a trombone playing in unison with the piano and the players reading the score over the shoulders of the pianist. The chords of the left hand are in the score, but the brass is not playing them. In the MONO mode, on the contrary, each instrument has its own part to play and the scores of the other instruments do not matter.

It is, in our opinion, fruitless to go further into the theoretical details of the MIDI configuration, for only practical use will really show up its effectiveness. In the meantime, we believe that the principal virtues of MfDf have been discussed from a practical point of view, which does not in the least pre-judge the richness (or poorness) of MIDI on the strictly musical plane...

Realization

Its realization, simplicity, and economy make the MIDI truly staggering. The compatibility it provides between products of different origin makes all the difference: communication is made possible where it was not before, and more flexible — and thus more efficient — where it was difficult before. And, of course, it also increases the turn-over of electrophonic businesses.

The more costly units, such as a dynamic touch keyboard, may be operated at the same time as several other units. Similarly, the microcomputer controlling the whole system contains mass storages such as floppies, from which the MfDf system may profit. Shared joy is double joy!

The fact that all information consists of logic bits makes it possible for it to be accessed more easily, more often, and at less expense than would be the case with buying new material.

Finally, there is another advantage the digital system has over the analogue and which is very much appreciated by musicians, and that is its precision. This is as good for pitch (no more problems with tuning, drift, and so on) as it is for rhythm and synchronization. ■

Did you know...?

A new museum, devoted to film and television, will take its place alongside drama, sculpture, fine art, and music on London's South Bank complex. Called the Museum of the Moving Image, it will open in 1987, with displays devoted to the cinema, television, and video, plus futuristic images in fibre optics and lasers.

The £7 million museum will be built on a 3000 m² plot next to the National Film Theatre. It will comprise twenty sections, plus a special exhibition, which will change every six to twelve months. It will cater for up to a million visitors a year and will be open up to twelve hours a day, seven days a week.

The museum will be no ordinary collection of static exhibits to be viewed silently: the visitor will be invited to experience and participate. There will be an operational TV control room overlooking a miniature studio which visitors can operate by themselves, as well as areas dealing with news and documentary. Museum goers will be able to watch an animation film being made, and there will be a place where children can spend an afternoon creating their own animated movies. There will be talks and lectures from actors, directors, and technicians, and there will be a library of related video material. ■

Over the past twenty years or so, the production and use of batteries have grown enormously. Whereas in the sixties their main use was in portable radios and torches, nowadays they are found in quartz watches, pocket calculators, hearing aids, portable computers, camera flash units, and many more.

Batteries consist either of primary, i.e., non-rechargeable, or of rechargeable cells. Primary batteries may be sub-divided into zinc-carbon, alkaline manganese, mercuric oxide, silver oxide, lithium manganese dioxide, lithium chromoxide, and zinc air types. The best known — and oldest — rechargeable battery is the lead-acid type, although nickel-cadmium batteries are catching up fast. As this article is concerned with the effect of batteries on the environment, it deals with primary batteries only, as these are disposed of by the million every day.

Zinc-carbon

Zinc carbon batteries are the least expensive, have the smallest capacity, and have a greatly varying capacity depending on the current. Their nominal e.m.f. of 1.5 V degrades linearly in use; when this has reached about 0.9 V, the battery should be thrown away.

Alkaline manganese

Alkaline manganese batteries are more expensive than zinc carbon types, but have a much better performance, particularly at higher currents and at lower temperatures.

Mercuric oxide

Mercury batteries offer a virtually constant voltage over their effective life. Moreover, they have a high energy density and good storage characteristics. Their output current is, however, limited at low temperatures.

batteries: a danger to the environment?

Mercury

Many primary batteries contain some mercury, albeit usually in very small quantities. Mercury is, of course, used in other electrical equipment as well: switches, mercury vapour lamps, and in the cathode of certain rectifiers. Compounds of mercury are highly poisonous, although several are used in medicine. An amalgam with cadmium, also used in dental fillings, is the alloy found in primary batteries. It is interesting to note that mercury — chemical symbol Hg — is the only metal that is liquid at room temperatures, whence its use in barometers and thermometers.

Mercury does not become inert in its natural state, is not affected by dilute acids, and only dissolves in hot oxidizing acids. The mercury contained in discarded batteries that each week land on refuse disposal dumps by the million remains stable and may, therefore, become an environmental hazard in years to come.

Zinc

Another element contained in primary batteries that may cause problems is zinc, but nowhere near as serious as mercury. This is because zinc burns in air, and combines with halogens and sulphur.

Alternatives?

Before the question as to alternatives to zinc and mercury can be answered, the characteristics of the various primary batteries should be considered. The table gives an overview of some of the properties of a number of primary batteries.

Lithium

Their very small size and extremely high energy density makes lithium manganese dioxide batteries ideally suitable for use in miniaturized electronic equipment. They are able to perform effectively over a temperature range of -20 °C...+50 °C, and have an exceptionally low rate of self discharge. 85 per cent of their capacity remains available after six years of storage at +20 °C. Lithium chromoxide batteries also offer a high energy density, low self discharge, and a wide temperature operating

Photograph by courtesy of Duracell.



range, but, in addition, maintain an e.m.f. of over 3.5 V with normal loads (lithium manganese dioxide >2.7 V), and have a design (storage) life of 10 years. Lithium batteries also have disadvantages in that they are more expensive than alkaline types and, because of their different output voltage of 3.0 V nominal, cannot simply be used as a substitute for 1.5 V batteries in existing equipment.

Silver oxide

The nominal e.m.f. of silver oxide cells is 1.5 V. Storage life is about 2 years at +20 °C; at the end of one year, about 90 per cent of nominal capacity remains available. Batteries of this type also perform well at low temperatures.

Zinc air

In zinc air cells, the reaction of zinc with

atmospheric oxygen in the presence of a catalyst is used to produce the electrochemical potential. The use of oxygen from the air means that the cell can be filled with nearly twice as much anode material, i.e., zinc, as, for instance, corresponding silver or mercury oxide cells. This gives zinc air cells a very high energy density and nearly double the life of silver and mercury cells.

From these considerations, it would appear that two types of primary battery might pose an environmental hazard: the mercury — self evidently — and the alkaline manganese. The latter appears not to be at first sight, and perhaps rightly as long as a single cell is considered. However, this type of battery is produced in growing numbers as a composite unit with a volume of from 10 to 100 times that of a single cell; in that case, the amount of mercury becomes a matter of concern.

It is clear from the foregoing that alternatives for both types, depending on application, are the silver oxide, the lithium, or the zinc air cell. In some instances, alkaline manganese units may be replaced by zinc carbon types.

Some properties of the most common primary cells
As far as the environment is concerned, the mercury cell is clearly potentially the most dangerous. As far as the energy density is concerned, the lithium and zinc air cells are the clear winners

cell type	chemical symbol	nominal emf per cell	percentage mercury	energy density mWh/cm³
zinc carbon		1.5 V	<0.01	120 190
alkaline manganese		1.5 V	1.0	200 300
lithium	Li/X	3.0 V	0	650 800
mercuric oxide	HgO/Zn	1.35 V	25 30	400 520
silver oxide	AgO/Zn	1.55 V	<1.0	550 650
zinc air	Zn/O ₂	1.45 V	<1.0	350 430
				650 800

Finally

If and when fewer mercury cells will be used, it is likely that more silver oxide cells will be produced to satisfy battery demands. Would it not be feasible for some enterprising concern to collect these cells when used and recycle the silver in them?

overload protection for electric drills

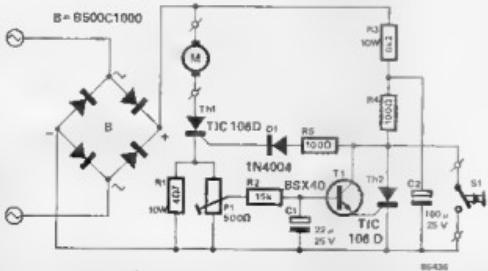
This circuit prevents the burning out of the motor of an electric drill through an overload. The mains voltage is transformed into

a pulsating direct voltage by a bridge rectifier. The motor of the electric drill forms the load of silicon-controlled rectifier (SCR) Th₁. Resistors R₃, R₅ and diode D₁ keep the SCR on as long as the current, I_M, through the motor does not exceed a given value. The motor current is monitored by resistor R₁; its maximum value depends on the setting of P₁.

If an overload causes I_M to exceed the maximum value, transistor T₁ switches on and triggers SCR Th₂. The gate circuit of Th₁ is then short circuited, and the motor is switched off.

Capacitor C₂ ensures that Th₂ is kept on until the circuit is reset by switch S₁. Resistor R₂ and capacitor C₁ form a low-pass filter which ensures that Th₂ cannot be triggered in error.

Preset P₁ allows the circuit to be used with electric drills rated between 50 W and 1 kW.



minivolt

Continued from page No. 12-33

T2 and R2. This discharge current (and, therefore, the discharge time) is determined by the input voltage, as described earlier.

Once C1 has discharged to the lower switching threshold of N1, C1 is recharged rapidly and the cycle repeats. The higher the input voltage the faster C1 will be discharged, and the higher the output frequency will be. This frequency is gated into the counters by the internal time base (shown in the dashed box in the circuit diagram). The time base really has three functions: gating the incoming frequency, blanking (turning off) the display during the count cycle, and resetting the counters 1000 µsec before the start of the count.

The duration of the positive portion of the waveform being produced by the time base must be 'spot on', otherwise

the unit will not be accurate. Therefore P1 is provided for full scale calibration of the unit. The timebase output has a very low mark to space ratio so that the count cycle is very short compared to the readout time. During this 'enable' time the output of gate N2 is high T3 is switched off, blanking the display (this is perceptible as a short blink). The reset pulse (the positive edge of the enable pulse) is passed via C3 to the counter section. Resistors R5, R6 set the voltage level at pin 9 of gate N3 and pin 13 of gate N4 between the switching thresholds of these Schmitt triggers. A positive pulse will now switch the gate output to '0' and a negative pulse will switch it to '1'.

The reset pulse will turn on T4 briefly, so that the outputs of N3 and N4 will both switch to '1'. T5 and T6 are turned off and the '100's' display (D7) switch it to '1'.

Positive pulses ... supplied by the 'carry' output (pin 5) of the decade counter IC2 at each transition from

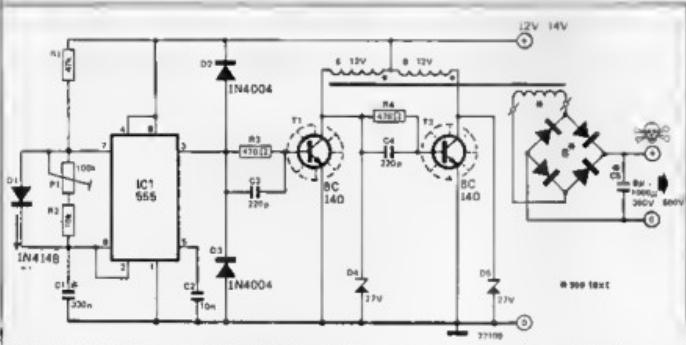
9 to 0, and resulting step is differentiated by C5 and R10.

The first time this occurs, N3 switches to '0'. This turns on T5, so that a '1' is displayed (segments b and c of the 'hundreds' display). C4 is still discharged, so the output of N4 is held at '1'.

However, C4 is now charged through R8 and T5. The next zero-to-one transition at the output IC2 (overflow) gives a second positive pulse. This time, the output of N4 does switch to '0', causing the display to read 'H' (for 'HELP'). At the same time IC1 and IC2 pins number 5 (display enable) change to low, inhibiting the readout by D5 and D6. As a result the D7 character 'H' is the total display.

Calibration

Apply a known voltage between 1 and 12 V to the input terminal 1 for the correct readout. Since the DVM only reads to 1.99 V, an external voltage divider must be added if higher voltages are to be measured.



This inverter circuit can be used to power electric razors, stroboscopes and flash tubes, and small fluorescent lamps from a 12 volt car battery. In contrast to the usual feedback oscillator type of inverter, the oscillator of this inverter is separate from the output stage, which allows easy adjustment of the oscillator frequency to suit different applications.

The oscillator circuit consists of a 555 timer connected as an astable multivibrator. The inclusion of D1 ensures that the duty-cycle of the squarewave output is maintained at about 50%. The output of the 555 drives the base of T1 which switches current through one half of the primary of the transformer. T2 is driven from the collector of T1 and thus switches current through the other half of the transformer winding on opposite half cycles of the drive waveform. Zener diodes D4 and D5 protect T1 and T2 from any high-voltage spikes generated by the transformer.

The voltage applied to the transformer primary is stepped up and the required high output voltage appears across the secondary winding. Depending on the application the secondary voltage may or may not be rectified.

Components

The transformer is a standard mains transformer with two identical secondary

windings or a single, centre-tapped secondary. This transformer is, of course, driven in reverse, i.e. the secondary becomes the primary and the output is obtained from the primary (which is now the secondary). It must be borne in mind that, since the inverter produces a squarewave output, the RMS secondary voltage and peak secondary voltage are identical. This affects the choice of transformer for different applications.

The required secondary voltage of the mains transformer is given by $U_s = \frac{U_m}{U_p} \times 12 \text{ V}$

where 12 V is the inverter supply voltage

U_m is the normal mains primary voltage of the transformer.

U_p is the desired peak secondary voltage.

An electric razor requires 240 V^{*} RMS = 240 V^{*} peak, so if a transformer with a 240 V primary is used the secondary windings should each be 12 V or a single 12-0-12 winding. For vibrator type (non-rotary) razors the oscillator frequency should be 50-60 Hz, so the value of C1 should be 330 n and P1 should be adjusted accordingly. Rotary razors are less critical of mains frequency.

When operated from the normal mains supply, fluorescent lamps receive a peak supply voltage of around 340 V, which enables them to strike reliably. The transformer secondary voltage should be calcu-

lated with this in mind, which means that secondary voltages of eight or nine volts will be suitable.

Fluorescent lamps can be operated with improved efficiency at frequencies greater than 50 Hz, and the transformer will also be more efficient. Choosing a value of 56 n for C1 RMS oscillator frequency may be set to around 250 Hz. At frequencies much higher than this iron losses make the transformer less efficient.

The current rating of the transformer depends upon the load. For electric razors and small fluorescent tubes up to 8 W, 500 mA secondaries will be adequate. Higher output powers may be obtained by choosing a suitable transformer, replacing T1 and T2 by higher power types and reducing the value of R3 and R4 (minimum 120 Ω).

To power strobos and flash tubes the output must be rectified and used to charge a reservoir capacitor, which should be of a type rated for high discharge currents. The bridge rectifier should be rated to suit the peak output voltage.

* U.K. only. Overseas readers substitute the appropriate local mains voltage.

play ball with Elektor!

Here is a circuit that will appeal to the inveterate gamblers among our readers. It is an electronic version of the pin-ball machine, but is not so versatile as the professional machines found in amusement arcades, bars, and other public places. But then, it is also much less expensive and does not gobble up all your money. The idea for the circuit is based on a study conducted in Las Vegas, which suggests that any money won is of less importance to most players than the fact of getting a reward for his or her skill in playing the machine.



by K. Diedrich

With reference to Fig 2, when the player presses S_1 , bistable N_5, N_6 toggles and this switches on oscillators $N_1 \dots N_4$. The resulting clock signal at pin 1 of IC₁ causes this circuit to commence counting. Inputs A, B, C, and D of IC₂ become logic low, and this starts the ball rolling! Accompanied by flashing lights and appropriate sounds, the imaginary ball rushes about, hitting pins galore, and finally disappears. The length of time it is in play can be extended by skilful use of switches S_2 and S_3 . The pins are represented by variously coloured LEDs, although D₃₀ and D₃₁ are on all the time. As soon as D₂₉ or D₃₂ lights, S₂ or S₃ should be pressed, as your skill indicates. If you have judged correctly, the ball travels back upwards and keeps the game alive. Possible positions of the pins (LEDs) are suggested in Fig.1.

Circuit description

Clock oscillator N₁ — see Fig.2 — enables speeding up or slowing down of the ball; its

frequency is controlled by N₂. Oscillators N₃ and N₄ affect the to and fro travelling of the ball; they drive two NAND gates, N₇ and N₈, which in turn provide logic levels to one of the inputs of XNOR gates N₉ and N₁₀. These latter gates invert the logic levels at inputs A and B of IC₂ at irregular intervals that depend on the setting of the relevant oscillator. If only the least significant bit LSB is inverted, the ball jumps one LED higher or lower, again depending on the relevant logic level. If input B is inverted, the ball travels two LEDs up or down. Oscillator N₂ controls the clock signal: it operates in an erratic manner. Its prime task is to switch T₁ on and off and thereby short-circuit C₂ or not in the process. The effect of this is that the clock is speeded up for a short time, which causes the ball to travel faster, just as in a professional machine. The tendency of the ball is, of course, to move downwards (prior to disappearing), so that at some time D₂₅ will light. The Q₁₅ output of IC₂ will then become active: transistor T₂ switches off, which resets bistable N_{5, N₆}; the clock oscillator then stops, and the

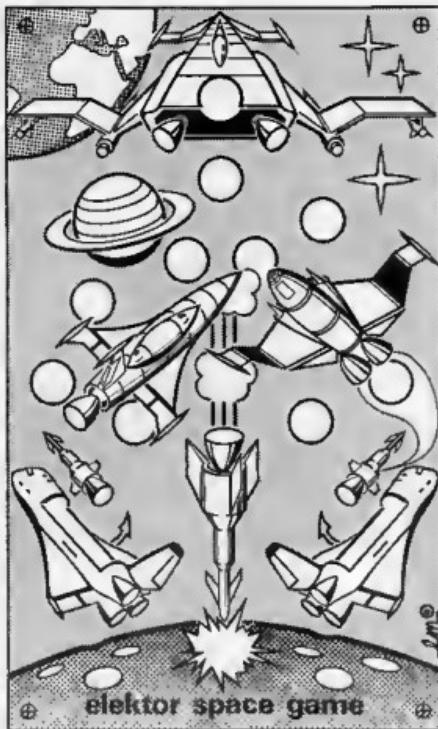


Fig 1 Layout of the indicator LEDs - see also Fig. 5

game is over. All this can, however, be prevented by rerouting the ball upwards with S_2 or S_3 . Note that these switches should only be pressed at the precise moment that D_{20} or D_{23} lights. If this is done skillfully, IC_1 is reset, and the clock oscillator continues to operate; if not, the ball is suspended and the last lit LED remains on. The Q_9 and Q_{12} outputs are not connected direct to D_{20} and D_{23} respectively, but via drivers T_6 and T_7 . The logic level present at the bases of these transistors is applied to NAND gates $N_{12} \dots N_{16}$.

When either S_2 or S_3 is pressed judiciously, N_{13} is provided with a 1 at its pin 9. Together with the 1 at its pin 8 (from Q_9 or Q_{12}), this results in a 0 at its output. This is inverted to a 1 by N_{14} , which is applied as a reset pulse to IC_1 via D_4 . IC_1 resumes counting and D_{21} lights again.

The logic 1 at the cathodes of D_8 and D_{10} is also applied to N_{15} , which then generates a 0 at its output. If S_1 or S_2 has been pressed timely, one of the inputs of N_{16} is 1. This means that T_3 remains on. Pin 1 of N_6 is then high, and the bistable remains set.

If S_2 or S_3 was not pressed timely, which means that the logic 1 from Q_9 or Q_{12} has already disappeared at the time of pressing, both inputs of N_{16} are high. The base of T_3 then becomes 0, and C_8 discharges slowly. After a short delay, the transistor switches off, and this pulls pin 1 of N_6 low. The bistable is then reset and the clock oscillator stops. The game is over!

The ball is put back into play with S_1 : IC_1 then receives a reset pulse, and the oscillators start as before.

To make the game even more realistic, a small loudspeaker has been added which provides the typical sound effects of a pinball machine. Every time N_7 or N_8 provides a logic 1, the leading edge is differentiated by one of four RC networks and applied to pin 1 of N_{17} via $D_5 \dots D_8$. The signal triggers the chain $N_{19} \dots N_{27}$. The frequency of oscillator N_{17} may be set as required by preset P_5 .

The rectangular signal is amplified by T_9 . The value of R_{14} has been chosen to give a suitable volume for most purposes; if more power is wanted, the value of the resistor

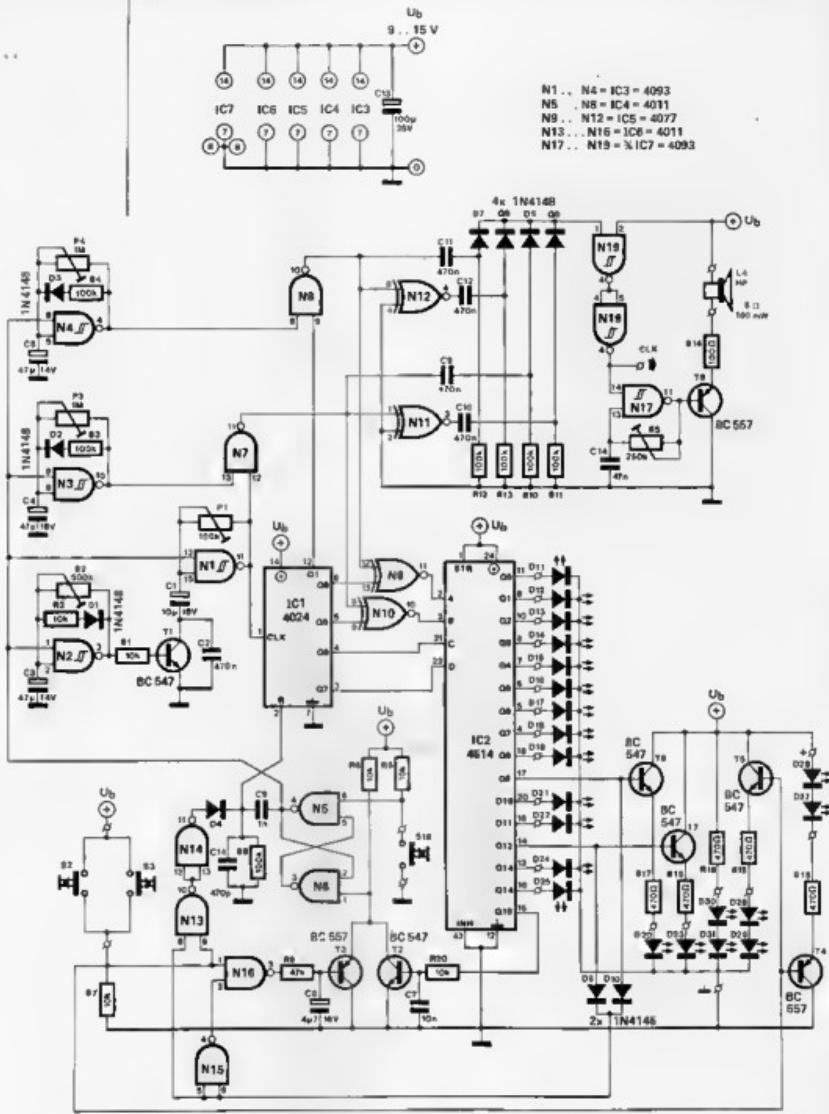


Fig.2 Circuit diagram of the pin-ball machine.

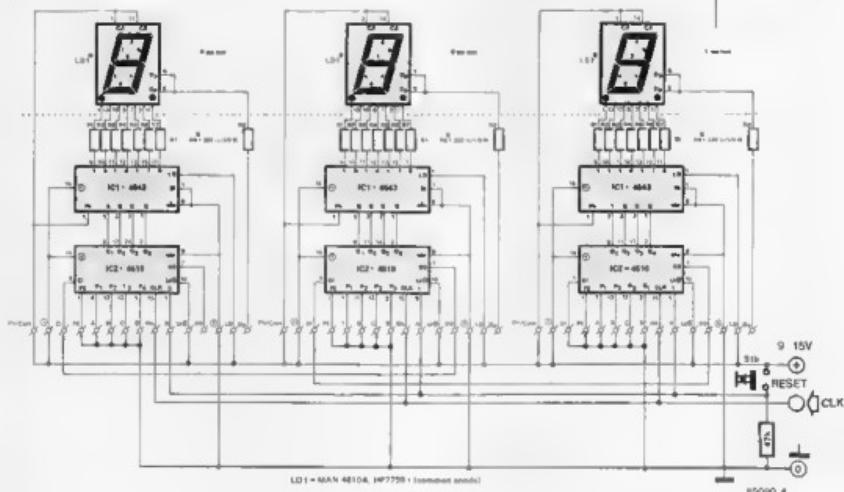
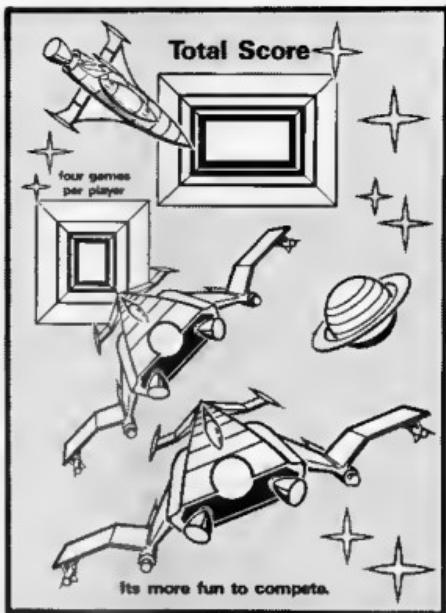
may be reduced, but not below about 50 ohms; its rating should then be increased to ½ W.

To ensure that the trailing edge of the pulse is also made audible, the output signal of N₇-N₈ is inverted by XNOR gates N₁₁ and N₁₂ and then differentiated.

The remaining presets may be set to individual taste, experience, and reaction

time by trial and error. The pin-ball will operate whatever their settings, because they all have a series resistance.

To use the pin-ball machine competitively, a counter and associated display is required — see Fig.4. The versatile counter circuit described in our April 1985 issue, P. 4-44, is ideal for this purpose. Note that if more digits than shown in Fig.4 are required,



these are simply added by connecting the power lines and the Co line of the previous section to the Ci of the added section.

Construction

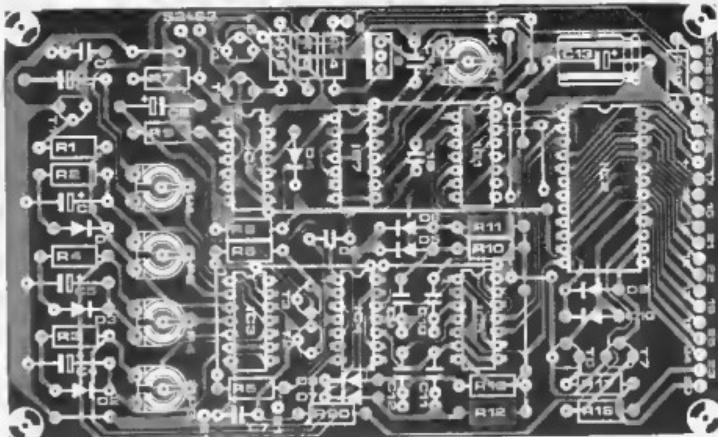
In the mechanical design of the unit, you can give your imagination free vent,

although a possible set-up is shown in Fig.3. Whatever enclosure is chosen, it must, of course, be large enough to house the PCB and it is advantageous to have the display section at an angle. The best position for S_1 is in the right-hand bottom corner of the front panel, while S_2 and S_3 are best fitted in the left- and right-hand side panels respectively near the front of the unit.

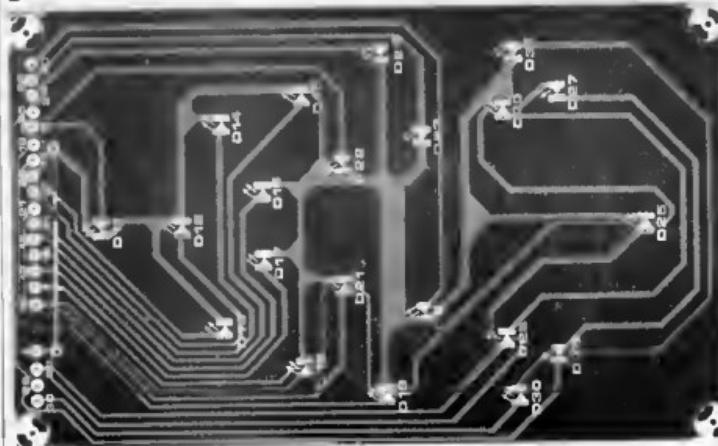
Fig 3 Suggested construction complete with points counter and associated display

Fig 4 Circuit diagram of the points counter and display — these were originally featured in our April 1985 issue

a



b



Parts list

Resistors*

R₁, R₂, R₅, R₇ = 10 k
 R₃, R₄, R₆, R₁₀, R₁₃ = 100 k
 R₉ = 47 k
 R₁₄ = 100 Ω (see text)
 R₁₅ = R₁₆ = 470 Ω
 P₁ = 100 k preset
 P₂ = 500 k preset
 P₃, P₄ = 1 M preset
 P₅ = 250 k preset

Capacitors

C₁ = 10 μF, 16 V
 C₂, C₉, C₁₂ = 470 n
 C₃, C₅ = 47 μF, 16 V
 C₄ = 1 n
 C₆ = 10 n
 C₇ = 4μF, 16 V
 C₈ = 100 μF, 25 V
 C₁₁ = 47 n
 C₁₅ = 250 p

Semiconductors*

D₁ = D₁₀ = IN4148
 D₂ = D₂₅ = LED; red
 D₂₆ = D₃₁ = LED; green or yellow
 T₁:T₂:T₃:T₄:T₅:T₆:T₇ = BC547
 T₈ = BD410
 IC₁ = 4024
 IC₂ = 4514
 IC₃:C₇ = 4093
 IC₄:C₈ = 4011
 IC₅ = 4077

Miscellaneous

S₁ = S₃ = spring-loaded push-button switch
 loudspeaker 8 Ω, 100 mW
 enclosure to individual requirements
 PCB 85090 1
 PCB 85090-2 (Indicator panel)

Please see page 1255
 for PCB artwork

The circuit is constructed on the printed-circuit boards shown in Fig.5. The indicator board serves also as decorative front panel (the decorations are not shown here, but are provided on PCB 85090-2 available through our readers' services).

If you want to provide the unit with its own power supply, this should be taken into account when planning the enclosure. The unit requires 9...15 V at about 100 mA. The power supply may, of course, be combined with that for the display section as shown on page 47 of our April 1985 issue. Where the display of Fig 4 is used, connect its clock input to pin 4 of N₁₀.

Did you know...?

Phoenix, the British Army's new surveillance system, contains a fully equipped pilotless aircraft for real-time targetting and battlefield surveillance. Apart from the small aircraft with its advanced avionics and infrared imaging equipment, the system comprises an air-to-ground data link, a mobile communications ground station, and logistics vehicles for launch and recovery. The air vehicle will have low radar, infra-red, and acoustic "signatures" to make it hard to detect. Its modular construction and small size make it easy for soldiers to assemble, launch, and recover.

Computers aid survival of rare plants

by Martin Redfern

There are about a quarter of a million different plant species in the world, but botanists estimate that, if man continues to exploit the natural environment at the present rate, one-sixth could be extinct before the year 2050. Many could disappear without ever being properly identified and without their potential for man being realized.

The International Union for the Conservation of Nature (IUCN) and the World Wildlife Fund (WWF) have responded to the emergency with a Plants Campaign, aiming to raise US\$4 million to protect the habitats and save individual plants. One of the problems is knowing exactly which plants are in danger and where they still survive. The IUCN Conservation Monitoring Centre (CMC) can provide some answers. It is based at Cambridge and publishes the Red Data Books on threatened plants and animals. The botanical section of the centre is at Kew Gardens in London, where plant enthusiasts of past centuries often brought their discoveries.

The CMC now operates an electronic database which scientists at Cambridge and Kew can update and expand each time new information is available. Apart from governments and organizations that are members of the IUCN, more than 2000 scientists worldwide are contributing information, together with researchers on 300 IUCN or WWF field projects.

Data Bank

Data on more than 14 000 threatened plant species have been entered in the computer store, both as key facts and as pages of descriptive text. In addition to a plant by plant analysis, there is information on the status of plants in different countries.

Researchers can ask questions of the database, such as: "Which plant species are under threat in Poland?" or "Are there any species of wild potato threatened with extinction?". There is also an inventory of protected areas such as national parks.

Plants that are particularly rare, or even extinct in the wild, sometimes survive in the 130 leading botanic gardens around the world. At the push of a button, it is possible to see how many gardens hold a particular plant, whether the specimens came from certified wild stock, and whether gardens

can provide seeds or duplicate plants. Botanists can tell at a glance which plants are held only at one or two gardens and which are widespread, and so priorities can be adjusted accordingly. The database actually discovered one plant thought to be extinct. *Sophora toromiro*, once a native of Easter Island in the Pacific, had been assumed extinct for 50 years until the computer traced specimens in the Gothenburg Botanic Garden, Sweden.

The activities of the Threatened Plants Unit at Kew are not just in the interests of science and the love of nature. Many endangered species may hold great economic potential for man, even if the potential has not yet been recognized. A good example is the Yicib (or Yehib) - a bush that used to be common in Ethiopia and Somalia. But famine, drought, and over-grazing have taken their toll.

Tasty Nut

The Yicib bears a tasty nut that is rich in protein. It was once a traditional food, grew wild, and was ideal for passing nomads. But the expanding population has taken all the nuts, leaving none to seed new plants. Even the bushes themselves have been used for firewood. Now, Yicib is on the IUCN's

list of the 12 most endangered plants. Another on the list - the African violet - has become the symbol of the Plants Campaign. In cultivation, it is an abundant houseplant, with world trade valued at US\$30 million per year. But in the wild it is restricted to a couple of mountain forests in Tanzania. Eighteen out of 20 species are unique to Tanzania and the commonest houseplant, *Saintpaulia ionantha*, was known only on the Usambara mountains, already badly degraded by man.

In 1983, Jon Lovett, a British botanist working for the WWF, found the species growing in the Uzungwa mountains. But a sawmill is under construction there with a view to logging 40 000 ha of the forest. The Plants Campaign has promised £60 000 to help turn part of Uzungwa into a nature reserve.

Through the CMC database, it has been possible to draw the world's attention not only to the plight of the African violet, but to that of other threatened species in the same area. Other houseplants, for example the African primrose, *Streptocarpus*, and the busy lizzie, *Impatiens*, have been bred from only a few wild species. There are many more that are hardly known and which could offer tremendous potential to horticulturalists. Others may yield new medicines or



Christine Leone and Stephen Droop, senior research officers at the Threatened Plants Unit, examine a *Saintpaulia ionantha*.

other products. Of 40 known wild species of coffee, ten are unique to Tanzania. Only three species have been used so far for cultivation. Coffee is one of Tanzania's main exports and the wild species could represent a valuable new resource.

Worldwide Network

In the future, the database at the CMC is to expand to include more information

on more plant species and will become part of a worldwide network of environmental data. Already, it is part of the Global Environmental Monitoring Service run by the United Nations Environment Programme (UNEP).

UNEP is now setting up an even bigger system called GRID, which will combine all the data into one huge computer network. Decision makers will then be able to find, from a single

source, information on such things as climate, soils, water resources, pollution, animals, and plants for any part of the world. With such knowledge of the full environmental implications, it should be possible to plan projects with greater care and concern for the natural world.

(LPS)

Moves towards a cashless society

by David Lascelles

First came cash, then cheques, and then credit cards. The next step along the way the world pays for its goods could consist of electronic blips and flashes.

As befits the computer age, bankers and retailers in many countries are studying push-button payment that could largely do away with paper transactions and revolutionize the meaning of money. But, like all revolutions, their deliberations are fraught with uncertainty, not least because the shopper may prefer to stick with good old fashioned notes and coins.

The new method goes by the odd name of EFTPOS, which stands for Electronic Funds Transfer at Point Of Sale. The idea is that the shopper pays for goods at a check out through a terminal which instantly transfers money from his or her bank account into that of the shop. No coins or paper slips are involved: only electronic messages whizzing between banks and terminals.

It is not as futuristic as it seems. Several countries in Europe, the Far East and North America already have small EFTPOS systems, most of them operated by chains of shops or petrol stations. But none has caught on in a big way and some did quite the opposite, conspicuously failing to appeal to shoppers.

Experimental Territory

However, EFTPOS received a big boost with the decision by leading English and Scottish clearing banks and retailers in January 1985 to set up what is likely to be the world's first nationwide system, with 250 000 terminals usable by 20 million people by the end of the decade. The United Kingdom is, in many ways, an ideal proving ground: geographically a small country with a large urban population, a sophisticated banking system, and a

small number of banks covering the whole country with their many branches. It is much more suitable than the sprawling United States of America or West Germany, with its multitude of small banks.

Not that the British have reached their decision easily. The banks dithered for years over whether EFTPOS was worth the massive investment — which will be several hundred million pounds — and whether people even wanted it. Nor could they agree with retailers how to share out the cost of installing the special terminals and hooking them up to bank computers via telephone lines.

On the other hand, banks were faced with a steadily rising tide of paperwork, with the proliferation of cheques and credit card slips, and they knew it would engulf them in the end unless they acted. So they have agreed to a pilot project in two year's time with big retail chains in Britain like Burton and Debenhams. This will pave the way to the fully fledged system they now want, once acceptable charge rates for transactions are set and technical details agreed with retailers.

The share-out of cost between banks and shops will be crucial to the success of the British experiment. To avoid an unseemly squabble, Deloitte Haskins & Sells, a leading accountancy firm, has been engaged to investigate the benefits of EFTPOS and its report will become the basis for cost allocation. There is still a danger, however, that the storeowners, large and small — who have deeper reservations about EFTPOS than do banks — will balk when they learn what their contributions are to be.

How It Works

EFTPOS comes in several forms. Usually shoppers have plastic cards which they insert into a special ter-

minal at the check-out point. Each shopper is identified by punching in a secret personal identification number, and the shop assistant keys in the amount of the transaction. The message goes down a dedicated telephone line to the shopper's bank where a computer checks that there is enough money in the account to pay the bill.

If there is, it debits the account and sends a message to the shop's bank to credit its account there. If there are not sufficient funds, the message comes back to the check-out counter that the customer cannot pay, and the transaction is cancelled. All this can be done in less than 20 seconds which is about the same as a cash transaction takes and is much less than writing out a cheque or credit card voucher.

For the banks, EFTPOS offers potentially huge gains in efficiency: the whole process is rapid and automatic, and cuts out vast amounts of paperwork and human labour. Ironically, however, the banks' own projections show that cheques and credit card slips will continue to grow even after EFTPOS is launched because of the burgeoning level of retail transactions. But bankers say that without EFTPOS, the growth of paper would be even faster. And perhaps by the 21st century, the tide will start turning against paper slip transactions.

Cheaper And Quicker

For the shops, EFTPOS offers speed and certainty of payment and, therefore, fewer bad debts. Because the money is transferred immediately, it will improve shops' cash flow. EFTPOS could also reduce the need to keep tills full of coins, and it will maintain a detailed record of transactions, including issuing receipts, which will help with accounting. All told, this should offset a good part if not all of

the cost of the system.

Bob Woodman of Burton, who heads the retail consortium's EFTPOS policy committee, said: "EFTPOS will be a cheaper and quicker way of making payment in shops."

Less clear, however, is what EFTPOS does for the shopper. The banks say it speeds up the check-out and saves the customer having to carry money around or sign cheques and credit card slips. On the other hand, EFTPOS means that a customer's bank account is debited right away whereas there is a period of credit if payment is by cheque or credit card.

However, some EFTPOS systems debit a credit card account rather than a bank account, and even those that are plugged into a conventional bank account can have inbuilt delays before the amount is actually debited.

Educating The Public

However, no matter whether the banks or the stores end up paying the lion's share of the cost, it will all eventually have to be passed on to the consumer. So unless EFTPOS produces genuine gains in efficiency, it could push up prices — and sharpen consumer hostility.

The banks hope people will take to the new equipment as quickly and easily as they did to cash dispensing machines, which took about three years. But they are making no assumptions. A big campaign to educate shoppers to the new technology is being developed, and video cassettes are already being circulated showing happy people using Britain's only sizeable existing EFTPOS system, that operated by the Clydesdale Bank at a small number of supermarkets and petrol stations in Scotland.

There is also the worry of security. Although EFTPOS operators can never guarantee 100 per cent safety, planners of the British system say the secret codes and equipment they use will prevent fraudsters tapping other people's accounts or altering EFTPOS messages. Generally, however, EFTPOS could help reduce robbery by cutting the use of cash and fraud by using an electronic system that should be very hard to crack.

Highly Sensitive Project

Banks expect the biggest users to be petrol stations, department stores, and supermarkets, but there is no reason why EFTPOS terminals should not be installed in other busy places like railway and airline terminals, travel agencies, and restaurants. Special equipment has even been designed for installation in small corner shops, although these would probably not be hooked up to central computers all the time.

EFTPOS will operate on British Telecom's (BT) telephone network with equipment and software made by IBM UK, subsidiary of the American computing giant. BT and FBM UK have been co-operating for some time on information systems in Britain, and made an EFTPOS proposal that was accepted. However, the award of business in this huge project is highly sensitive because of the large sums of money and jobs involved, and the British Government is keen to see other suppliers come forward when the system gets under way.

Britain's largest indigenous computer company, International Computers Ltd (ICL), will probably play a role, as will companies in the United States of America such as NCR, a leader in high

technology banking hardware. Several European countries are also interested, particularly France where EFTPOS systems have been in operation for a number of years but have never been pulled together nationally like the British scheme.

Helpful To Everyone

An important consideration for the designers of the system is the danger of being accused of setting up a cartel. Britain's Office of Fair Trading, which watches out for signs of excessive collaboration between competitors, is keeping a close eye on EFTPOS and is being consulted by the banks as they go along.

David Robinson, general manager of Williams & Glyn's Bank, who chairs the clearing banks' EFTPOS policy committee, said: "We are all aware of the complex work that lies ahead but are determined that in developing the system and network, the right balance will be struck between cooperation and competition so that benefits will be shared among all the participants." While the banks will be operating the system together, they intend to market their EFTPOS products individually. Competition should produce variations in service. Some banks may promise customers longer delays before purchases are debited, in effect giving them credit. Others may charge less for EFTPOS accounts than their competitors, or build extra services into them such as credit cards and overdrafts.

It will be a good ten years, however, before anyone can say that EFTPOS is the system of the future, and the British experiment will doubtless be closely watched all round the world.

(LPS)



A customer hands her bank cash card to the attendant at a supermarket check-out for authorization of payment by the Clydesdale Bank in Scotland via a computer terminal

high-resolution colour graphics card - 3

The third instalment of an article describing a 512×512 or 512×256 pixel, black & white or colour, graphics card.

by P Lavigne &
D Meyer

Circuit description

Address decoding

The eight most significant address lines, $A_8 \dots A_{15}$ in Fig. 15, are applied to the P-inputs of 8-bit comparator IC₁. The Q-inputs of this IC are polarized by resistors $R_1 \dots R_8$ and switches $S_1 \dots S_8$. When the most significant address byte on the bus is the same as the binary word programmed by the user with $S_1 \dots S_8$, output $P=Q$ of IC₁ goes low, which enables IC₂ to read address lines $A_4 \dots A_7$. Since address line A_7 is tied to enable input G_{2A} of IC₂, this circuit is active only for addresses between XX_{4Y} and XX_{5Y} , where XX is defined by $A_8 \dots A_{15}$ of IC₁ and Y by IC₃. Note that the presence of S_2 on enable input G_1 of IC₂ ensures that the address decoding is synchronized with the signals of the 6502.

Of the eight outputs of IC₂, only two are used, each of which defines a block of sixteen addresses. One activates the GDP's E(enable) input so that this is decoded between XX_{4S} and XX_{5P} ; the other enables IC₃, which deals with the sixteen bytes between XX_{4S} and XX_{5P} . The first address used in this block is XX_{64} . Presenting the R/W(read/write) line to input A_6 of IC₃ (low for write; high for read operations) allows some increase in efficiency. Two different decoding signals are obtained at the same address, depending on whether the operation in progress is a read or a write. This means that when XX_{64} is written, it is input to IC₁₂, but when XX_{64} is read, IC₁₃ is accessed.

At address XX_{45} (XX is user-defined), is write-only register IC₆. Read address XX_{45} is not used. Address XX_{45} is the location of write-only register IC₁₁. Once again, this register's read address is not used. When the CDP (IC₅) is active, associated data buffer IC₄ is also active. The data transfer direction is from data bus to GDP for writing and from GDP to data bus for reading. This is defined by the R/W line from the 6502, which is applied to pin 1 of IC₄. The other registers on the graphics card communicate direct with the data bus. The reason for this will be considered later. The address decoding is summarized in Table 3.

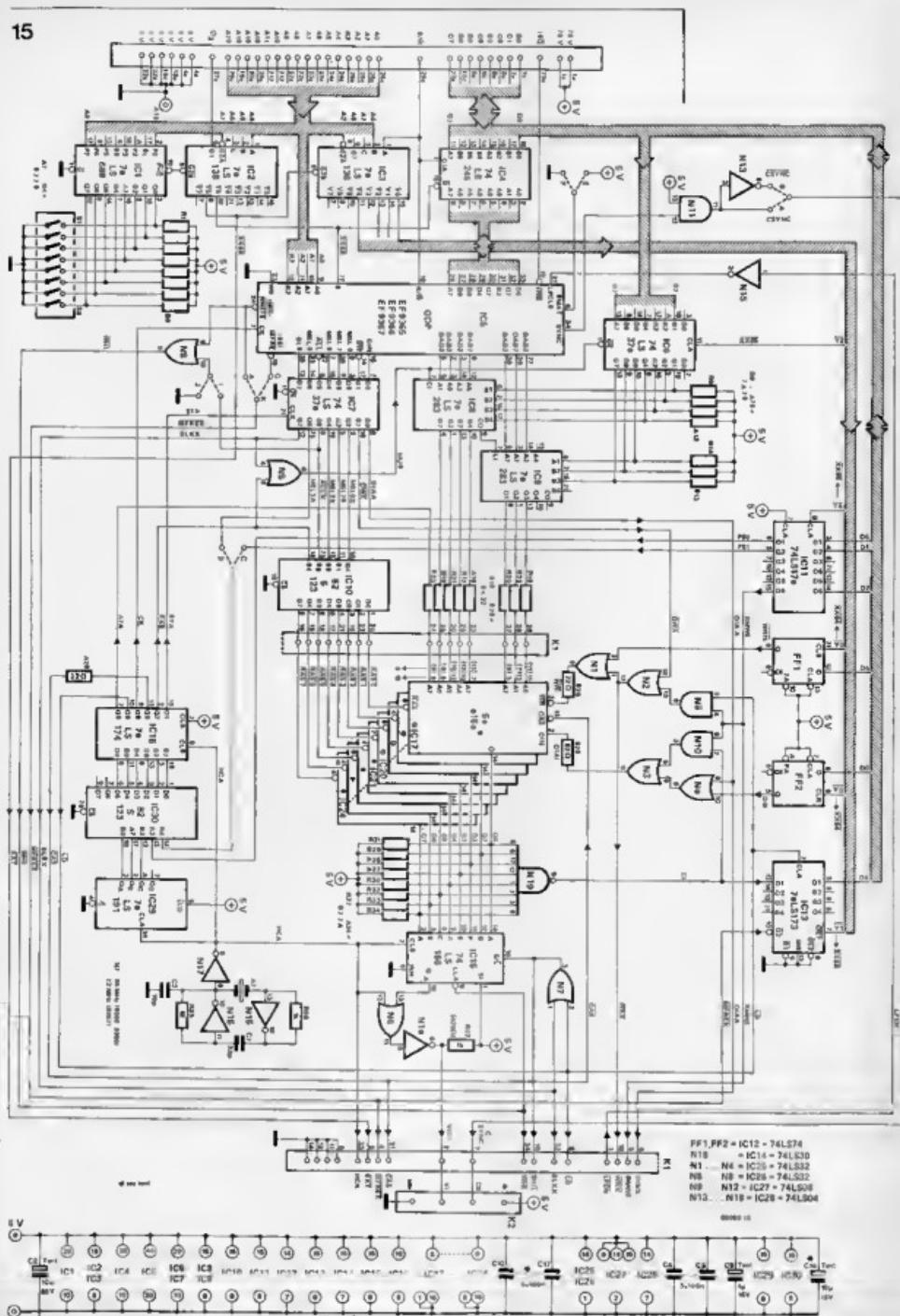
GDP and control signals

The GDP, with its eleven addressable

registers that are accessible from the micro-processor bus, is the heart of the circuit. Pins DAD₁...DAD₆ output the addresses of bytes that have to be accessed for reading (display), writing, or refreshing. As it happens, the first word to appear on these pins is $A_8 \dots A_6$, i.e., the address line for the RAM (RAS). The second word output is $A_8 \dots A_{14}$ of the RAM. Initially, consider the circuit as if IC₆ and IC₉ do not exist, and the DAD outputs are connected direct to inputs $A_6 \dots A_8$ of the memory. The timing for the entire card is controlled by clock CK. This clock is derived from the dot-clock generated by the quartz oscillator based on $N_{16} \dots N_{18}$. The frequency of this oscillator is 12 MHz in the EF9367, and 14 MHz in the EF9368, which is manifested by a smaller image in the former than in the latter. The high clock — HCK — signal times output shift register IC₁₅ direct. Apart from this, it is also fed to IC₂₉, a counter that continually repeats all possible binary configurations from 7 to 0 on its Q₀...Q₂ pins. This provides a cycle of eight clock pulses (= eight pixels = one byte), which establishes signals CK, RAS, CAS, STR, and A_7 via PROM IC₃₀. The three least significant address lines of this PROM are controlled by IC₂₉, so that the addresses from 7 to 0 are scrolled continually.

The most significant address lines are controlled either by PS₆ and PS₁, or by PS₆ and MSL3X. In the sequential scanning mode, PS₆ and PS₁ allow 4 × 8 different addresses in the PROM to be accessed. The signals in these four blocks are identical, with the exception of A_7 . In the interleaved mode, MSL3X replaces PS₁, and PS₆ takes care of the switching between the two high-resolution pages in the memory. The signals output by IC₃₀ are synchronized to the HCK signal via six bistables contained in IC₁₆. A complete listing of the contents of the PROM is given in Table 4. The timing diagram of Fig. 16 shows the HCK, RAS, CAS, STR, and LD signals — which are independent of the page selected — and the A_7 signal, which is determined by the condition of lines PS₆ and PS₁ or MSL3X. When CK is high, the line addresses are enabled by RAS; when it is low, the column addresses are enabled by the CAS signal. Whereas CAS is applied direct to the memories, RAS is not, because, as has been stated before, there must be some means of

Fig 15 Circuit diagram of the black-and-white version of the graphics card. Note that the pin connections of memories IC₁₇...IC₂₄, marked o, are not the same as those of memories IC₂₁...IC₂₄, marked ▶. This arrangement merely facilitates the design of the printed circuit and has absolutely no effect on the operation of the devices



A15	A8	A7	A6	A5	A4	A3	A2	A1	A0	R/W	address	register
P=0		0	0	0	x	x	x	x	x	x	XX00...XX0F	
		0	0	1	x	x	x	x	x	x	XX10...XX1F	not used
		0	1	0	x	x	x	x	x	x	XX20...XX2F	
		0	1	1	x	x	x	x	x	x	XX30...XX3F	
		1	0	0	x	x	x	x	x	x	XX40...XX4F	
		1	0	1	x	x	x	x	x	x	XX50	
		1	0	1	1	1	1	1	1	x	XX5F	GDP registers
		1	1	0	0	0	0	0	0	x	XX60	
		1	1	0	0	0	0	1	0	x	XX61	not used
		1	1	0	0	0	1	0	0	x	XX62	
		1	1	0	0	0	1	1	0	x	XX63	
		1	1	0	0	0	0	0	0	x	XX64	write: IC12
		1	1	0	0	0	0	0	1	x	XX64	read: IC13
		1	1	0	0	0	0	1	0	x	XX65	write: IC6
		1	1	0	0	0	0	0	0	x	XX66	read: not used
		1	1	0	0	0	0	0	1	x	XX67	hardware registers
		1	1	0	0	0	0	0	0	x	XX67	read: not used
		1	1	0	0	0	0	0	1	x	XX67	read: not used

Table 3 Truth table of the address decoding.

Table 4 The signals shown in Fig. 16 are generated during a read cycle uninterrupted by one of the eight address blocks of PROM IC₃₀. Whatever the block concerned (and this depends on which page has been selected to fill the screen), reading takes place from the most significant to the least significant address, e.g., 07 06 05 04 03 02 01 00 07 06 ... 01 00 07, etc.

discriminating collective from individual addressing. Therefore, the RAS pulse is combined with the ALL and MSL₁...MSL₂ signals. ALL is, of course, low to indicate collective memory access. The MSL₁...MSL₂ lines specify which of the eight bits in a byte is accessed. A second PROM, IC₁₀, is used for the decoding of the RAS, ALL, and MSL signals. Its contents are listed in Table 5, which shows that outputs RAS₁...RAS₇ are activated together only if both RAS and ALL are active, i.e., low, simultaneously. When RAS alone is low, the output that is activated is determined by MSL₁...MSL₂. Applying the RAS signal to a dynamic

memory IC not only enables addresses A₈...A₁₅, but also, in combination with CAS, addresses A₈...A₁₅. The result is that selecting RAS for one eighth of every cycle selects one bit from every byte. A CAS applied to a memory IC that has not already received a RAS has no effect.

The leading edge of the STR signal activates buffer IC₇, which toggles the levels of the MSL, ALL, BLK, DIN, and DW lines at the start of each cycle. These logic levels are only active for a much shorter time than the period of the CK signal: hence the need for an intermediate register.

The function of N₅, IC₆, IC₈, and IC₉ will be discussed later.

The memory and its peripherals

The memory on the mother board consists of eight Type 4164 (64Kx1 bit) ICs. These have a common CAS line, but separate RAS inputs. Address lines A₈...A₁₅ are controlled by the GDP, but A₇ is driven by IC₃₀ via IC₃₁.

Every address appearing on multiplexed address lines (A₈...A₁₅) + A₇ refers to a complete byte. If only one of the eight RAS lines is active, a single bit is selected. Each of the Q₀...Q₇ lines of the memory may have one of two outputs. In collective addressing, these lines are all active when shift register IC₁₅ is being loaded. The LD signal is applied to the SH/L (shift/load) input of IC₁₅ via N₇, so that the shift register gets loaded at the end of every cycle of IC₃₀; but, because BLKX is fed to the same input, the register cannot be loaded outside the display window. If the BLKX signal were removed, the GDP would manipulate the memory at the edges of the screen, but this is not within the purposes of this article.

The Q_H output of IC₁₅ supplies the video signal obtained from the contents of the memory. If two successive bits in a byte are high, the video signal remains high until the end of the second bit. This serves to reduce flicker on the screen, and is also the reason for routing the signal via gate N₆. This gate is triggered by the clock and compensates for any excess energy — see Fig. 17. The drawback of this arrangement is the need for a much larger bandwidth than that of a

PROM 82S123 (IC30)											
PSI	PSA	QC	QB	QA	ADDRESS HEX	N.C.	A7	LD	CAS	RAS	DATA HEX
R4	R3	R2	R1	R0	D7-D6	D5-D4	D3-D2	D1-D0	STR		
0	0	0	0	0	00	0	0	0	1	1	0
0	0	0	0	1	01	0	0	0	0	0	00
0	0	0	1	0	02	0	0	0	0	0	00
0	0	0	1	1	03	0	0	0	0	0	00
0	0	1	0	0	04	0	0	0	0	0	00
0	0	1	0	1	05	0	0	0	0	0	00
0	0	1	1	0	06	0	0	0	0	0	00
0	0	1	1	1	07	0	0	0	0	0	00
0	1	0	0	0	06	—	—	—	—	—	—
0	1	0	0	1	07	—	—	—	—	—	—
0	1	0	1	0	08	—	—	—	—	—	—
0	1	0	1	1	09	—	—	—	—	—	—
0	1	1	0	0	0B	—	—	—	—	—	—
0	1	1	0	1	0C	—	—	—	—	—	—
0	1	1	1	0	0D	—	—	—	—	—	—
0	1	1	1	1	0E	—	—	—	—	—	—
0	1	1	1	0	0F	—	—	—	—	—	—
1	0	0	0	0	10	—	0	1	1	0	0
1	0	0	0	1	11	—	0	0	0	0	20
1	0	0	1	0	12	—	0	1	0	0	30
1	0	0	1	1	13	—	0	0	1	0	30
1	0	1	0	0	14	—	0	1	1	1	0
1	0	1	0	1	15	—	0	0	1	1	0
1	0	1	1	0	16	—	0	0	1	1	0
1	0	1	1	1	17	—	0	0	1	1	0
1	1	0	0	0	18	—	0	1	1	0	0
1	1	0	0	1	19	—	0	0	1	1	0
1	1	0	1	0	1A	—	0	0	1	0	0
1	1	0	1	1	1B	—	0	0	1	0	0
1	1	1	0	0	1C	—	0	0	1	1	0
1	1	1	0	1	1D	—	0	0	1	1	0
1	1	1	1	0	1E	—	0	0	1	1	0
1	1	1	1	1	1F	—	0	0	1	1	0

page 0

page 1

page 2

page 3

typical monitor.

In selective accessing, all the RAM outputs are inactive (forced high by resistors $R_{27} \dots R_{32}$), except when the RAS line is active. The output of NAND gate N₁₉ is low when the addressed bit is high (because the other seven bits are also high), and high when the addressed bit is low. The logic signal on the SI line is, therefore, the converse of the addressed bit. The bit is loaded into register IC₁₃ and is read by the host microprocessor via the data bus, D₈, at address XX₆₄. Note that the bit is loaded into register IC₁₃ only when the pulse enabling the LD signal arrives and MFREX is active, indicating that the selected bit originates from the coordinates fed to the GPD by the microprocessor.

The SI signal is also fed to the colour selection circuit containing the RMW logic already described.

Writing to the screen memory

The screen memory can be written to only when the DW line is activated by the GPD. The write signal is applied to the WRITE pin of the RAMs when the WRIS (write I select) line is activated to select memory plane 1 in the colour mode. In the monochrome version, the WRIS line is active continuously. Whether the DW signal is applied to the RAM depends on the logic level output by AND gate N₉, which is part of the RMW circuit. Initially, assume that this output is low and that WR is, consequently, activated by the DW signal.

The data to be written into the memory appears on the DINX line. It can be led to RAM input D₈ via N₃ and N₄ only in combination with the level on the DIS (data I select) line and the output of AND gate N₁₀. When the latter gate (RMW logic) outputs a low level, and DINX is high, the GPD tends to quench the pixel in question. The DIS line, whatever its state, can then change nothing: the only external method of preventing the pixel being dimmed is taking the WRIS line in IC₁₂ high, which disables the writing to plane 1.

When DINX is low, the GPD tends to light the relevant pixel. Should the colour combination demand that the pixel be dark (e.g., when the pen and paper colours are different), the DIS line must be taken high while WRIS is active. This is of importance for the colour facility only. It is essential to include this from the start, however, because it cannot be added at a later stage — see Table 6. In the read-modify-write circuits — Fig.12 and 13 — gates N₁ and N₄, connected to register IC₁₀, are used to select the colours. The other gates, N₂, N₃, N₉, and N₁₀ are associated with the RMWS line provided by register IC₁₁. When this line is low, it is as if the four gates do not exist; when it is high, however, the circuit is in the RMW mode. Here again, when the GPD tends to quench a pixel (DINX = high), it cannot be stopped, except when the colour select logic disables the writing to one or more memory planes. The combination of RMWS and LD signals disables writing in the RMW mode, except at the precise moment when the bit

16

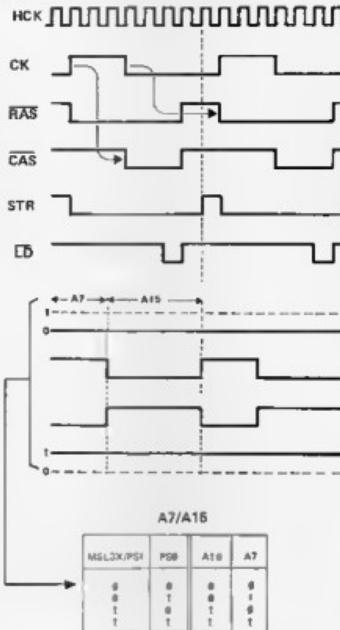


Fig.16 This diagram shows that the timing of the memory activating signals is of fundamental importance. Note that the active edges of the RAS and CAS signals are determined respectively by the trailing and leading edge of the clock signal. The bottom part gives the four possible logic combinations at A7. Note that these combinations are exclusive and cannot exist simultaneously.

Table 5 PROM IC₁₀ is not read cyclically like IC₂₀, since its role — when RAS is low — is to activate all lines RAS₀ .. RAS₇ when ALL is active and to deactivate them one after another when ALL has ceased to be active — the latter in logic combination with line MSL.

PROM 82S123 (ICt01)																
RAS	ALL	MSL2	MSL1	MSL0	ADDRESS	HEX	D7	D6	D5	D4	D3	D2	D1	D0	DATA	HEX
0	0	0	0	0	00	00	0	0	0	0	0	0	0	0	00	00
0	0	0	0	1	01	01	0	0	0	0	0	0	0	0	00	00
0	0	0	1	0	02	02	0	0	0	0	0	0	0	0	00	00
0	0	0	1	1	03	03	0	0	0	0	0	0	0	0	00	00
0	0	1	0	0	04	04	0	0	0	0	0	0	0	0	00	00
0	0	1	0	1	05	05	0	0	0	0	0	0	0	0	00	00
0	0	1	1	0	06	06	0	0	0	0	0	0	0	0	00	00
0	0	1	1	1	07	07	0	0	0	0	0	0	0	0	00	00
0	1	0	0	0	08	08	1	1	1	1	1	1	1	0	FE	FE
0	1	0	0	1	09	09	1	1	1	1	1	1	1	0	FD	FD
0	1	0	1	0	0A	0A	1	1	1	1	1	1	1	1	F7	F7
0	1	0	1	1	0B	0B	1	1	1	1	1	1	1	1	EF	EF
0	1	1	0	0	0C	0C	1	1	1	0	1	1	1	1	DF	DF
0	1	1	0	1	0D	0D	1	1	0	1	1	1	1	1	BF	BF
0	1	1	1	0	0E	0E	1	0	1	1	1	1	1	1	7F	7F
0	1	1	1	1	0F	0F	0	1	1	1	1	1	1	1	FF	FF
1	0	0	0	0	10	10	1	1	1	1	1	1	1	1	FF	FF
1	0	0	0	1	11	11	1	1	1	1	1	1	1	1	FF	FF
1	0	0	1	0	12	12	1	1	1	1	1	1	1	1	FF	FF
1	0	0	1	1	13	13	1	1	1	1	1	1	1	1	FF	FF
1	0	1	0	0	14	14	1	1	1	1	1	1	1	1	FF	FF
1	0	1	0	1	15	15	1	1	1	1	1	1	1	1	FF	FF
1	0	1	1	0	16	16	1	1	1	1	1	1	1	1	FF	FF
1	0	1	1	1	17	17	1	1	1	1	1	1	1	1	FF	FF
1	1	0	0	0	18	18	1	1	1	1	1	1	1	1	FF	FF
1	1	0	0	1	19	19	1	1	1	1	1	1	1	1	FF	FF
1	1	0	1	0	1A	1A	1	1	1	1	1	1	1	1	FF	FF
1	1	0	1	1	1B	1B	1	1	1	1	1	1	1	1	FF	FF
1	1	1	0	0	1C	1C	1	1	1	1	1	1	1	1	FF	FF
1	1	1	0	1	1D	1D	1	1	1	1	1	1	1	1	FF	FF
1	1	1	1	0	1E	1E	1	1	1	1	1	1	1	1	FF	FF
1	1	1	1	1	1F	1F	1	1	1	1	1	1	1	1	FF	FF

collective addressing

selective addressing

no addressing

to be changed is output by N_{19} — see Fig.16. The possible combinations of RMW logic in the monochrome mode are shown in Table 2. Further possibilities will be discussed later.

Scroll

The scroll logic consists of OR gate N₅, register IC₆, and high-speed 4-bit adders IC₂ and IC₃.

The manner in which the GDP relates the addresses on the screen to the memory addresses has already been dealt with. Since the GDP has not a scroll function (which is of particular interest in alphanumeric applications), the vertical addresses provided by the GDP must be modified. This is effected by the read-modify-write circuits.

There are two suitable types of scroll: one changes the screen contents with respect to the memory contents, and is quite complex; the other, which is much simpler, makes use of the visual effect of an endless drum revolving in front of the viewer. The latter type is used in the present card.

The vertical addresses (*y*-axis) are present during part of the addressing cycle only, since they are multiplexed with the horizontal addresses (*x*-axis). The latter are not modified, because this would result in horizontal scroll or a combination of vertical and horizontal scrolls.

Instead of demultiplexing the addresses, a basic characteristic of binary logic is used.

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Adders IC₈ and IC₉ receive the GDP address bits on their A-inputs, while their B-inputs accept a 7-bit binary word that is added to the A-word. The sum, which appears at the Q outputs, is either the unchanged horizontal address or the modified vertical address needed for the scroll. The 7-bit word, provided by IC₈, is determined by the software, and is based on the position of the cursor relative to the bottom of the screen.

The horizontal and vertical addresses, which follow each other at pins DAD₀ . . . DAD₆, are demultiplexed by N₅. This gate combines two signals: BLXK, which is active (high) outside the display window; and RAS, which enables the horizontal addresses. The resulting MUX signal controls the OE (output enable) circuit of IC₆; the outputs of this chip are high impedance when the device is inactive. The MUX signal is also applied to the CI (carry in) pin of IC₅; when it is high, the word fed to the B inputs of the adders is 11111111 (because of resistors R₁₀ . . . R₁₅). In this state, anything input to the A inputs of the adders appears unchanged at their Q-outputs. The MUX line is, therefore, kept high when no addition is required, as for positions outside the display window, and for horizontal addresses within the window that must not be modified.

The BLKX signal disables the adders outside the window, while inside the window, for vertical addresses only, they are enabled by RAS.

The procedure described may seem somewhat contradictory, but this is only apparent, because the purpose of a correctly specified RAS signal is the enabling of horizontal lines. The horizontal addresses are seen by the RAMs in the state they have on the trailing edge of RAS; this is one of the characteristics of dynamic RAMs. The logic levels output by the adders are, therefore, exactly as input to A when RAS goes low. The horizontal addresses are unchanged, but the vertical addresses appearing on the A inputs will be added to the word fed to the B inputs. When IC₆ and IC₂ are returned to the bypass mode (by RAS reverting to 1 at the end of the addressing cycle), the modified vertical addresses are enabled by the CAS signal.

A final note about register $1C_5$: when this contains FF_{HEX} (=]]]) (1111), both vertical and horizontal addresses remain unchanged. ■

Table 6 Some examples of logic combinations of the colour select lines when the read-modify-write mode is disabled.

write enable signals on color planes						data signals on color planes			GDP signals		J	
RMWS	R	G	B	I	R	G	B	I	DWX	DINX	PIXEL	
0	X	X	X	X	X	X	X	X	1	X	no write operation	
0	1	1	1	1	X	X	X	X	0	X	writing not allowed on this pixel	
0	0	1	1	1	X	X	X	X	0	1	turn off red dot; no change on green, blue and I planes	
0	0	0	1	1	X	X	X	X	0	1	turn off red and green dots, no change on blue and I planes	
0	0	0	0	0	X	X	X	X	0	1	turn off all dots	
0	0	0	0	0	0	1	0	1	0	0	turn on red and blue dots, turn off green and I dots	
0	0	1	0	0	1	X	1	0	0	0	turn off red and blue dots, turn off 1 dot, no change on green plane	
0	1	0	0	0	X	1	0	1	0	0	turn on blue dots; turn off green and I dots; no change on red plane	
0	0	0	0	0	1	1	1	1	0	0	turn off all dots	

Part 4 will appear in our January 1986 issue.

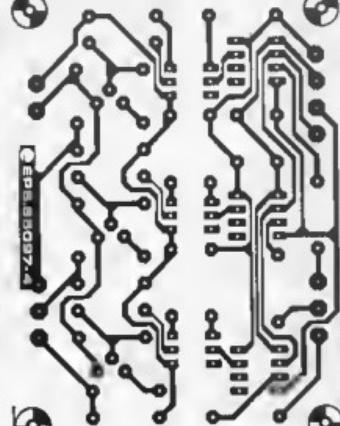
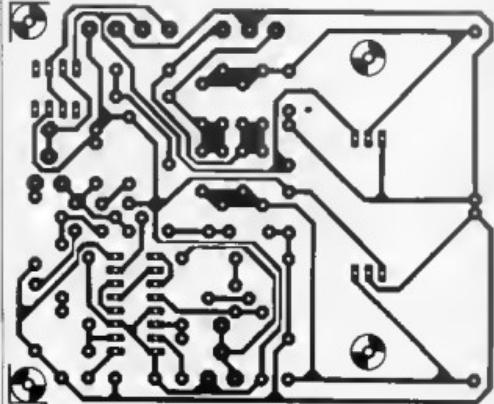
Fig.17 When a TV receiver is used instead of a monitor, the signal provided by the arrangement at the right gives better results than that at the left, because the energy is then distributed better between adjacent and isolated lighted pixels.

17

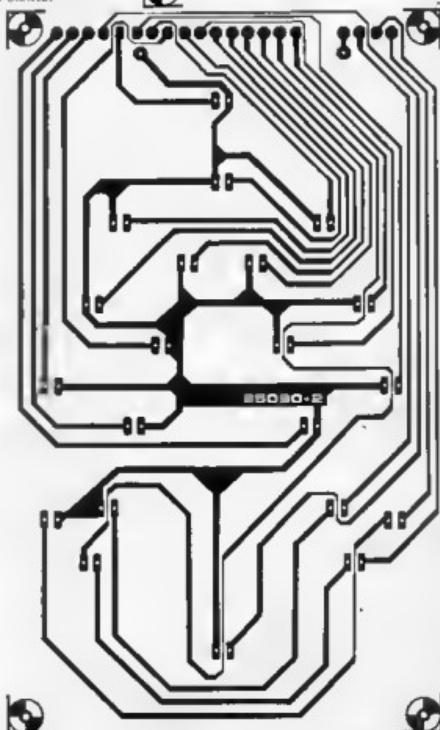
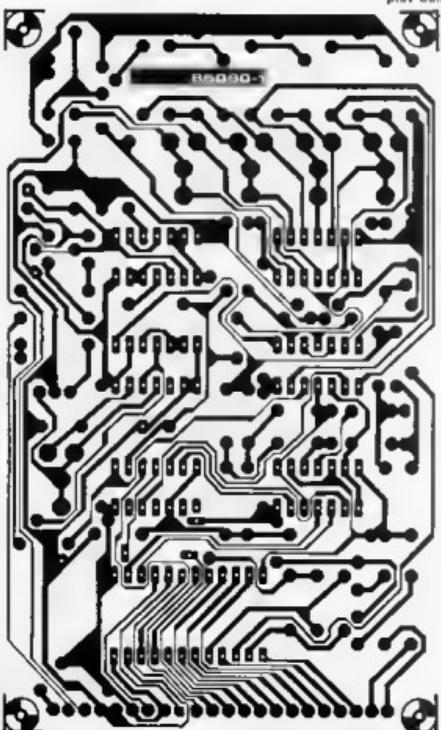


stage lighting II

PCB Track Patterns For Play ball-with Elektor and Stage lighting II



play ball with elektor



Ludus was conceived as a teaching aid in reading and writing classes, enabling the student to quickly learn, for example, the distinction between upper and lower case letters. The unit compares keyed-in given answers (yes/no or right/wrong) with previously programmed correct ones. It is therefore eminently suitable for use wherever a simple distinction between yes or no is to be made for a small outlay.

ludus

programmable
learn-and-play
unit

H. Rehbock

The unit provides eight cycles of twelve questions each, that is a total of ninety-six questions. When all twelve questions in a cycle have been answered correctly, a light begins to flash. It has been found that this type of reward has a strong motivating effect on the user.

The relative simplicity of the circuit limits the questions to two-choice ones which of course increases the chances of a 'good guess'.

The answer to each question posed is given by pressing either of the two keys, L(left) or R(right). This answer is compared with that previously stored in a register by means of the same two keys. If the two are the same, a point counter advances one step. Resetting is effected by pressing the reset switch S5 or the input keys simultaneously.

operation

When input keys S2 and S3 are pressed, debounce flip-flops N1/N2 and N3/N4 are actuated; when the switches are released, the flip-flops return to their quiescent state. The output state of gates N2 and N4 is compared in gates N5 and N6 with outputs Q and \bar{Q} of an 8-bit serial shift register, IC2. If the outputs of N2 and Q are both logic 1 (which means that switch S2 — left — was pressed correctly), the output of N5 goes logic low. Gate N8 then imparts a 1 to input B of monostable MMV2 which in turn triggers point-counter IC5. The same happens when the output of N4 and \bar{Q} are both 1.

Task counter IC4 is triggered by monostable MMV1 and counts one up every time an input switch is pressed. The monostable is triggered at input B by the leading edge of the pulse coming from N1 or N3 via gate N7. The outputs of N1 or N3 are 0 when S2 or S3 respectively are pressed. Apart from the trigger pulses for the point and task counters, the two monostables provide the clock pulse for IC2 and the control signal for the result indicator lamp Lal.

The time determining elements are C8/R14/D1 (MMV1) and C9/R15/D2 (MMV2). The trailing edge of the 20 μ s pulses at output \bar{Q} triggers the ap-

propriate counter. At the same time, switch S4b connects a 0 to input A of MMV2 which enables the monostable to react to a leading edge (from N8) at input B.

When MMV1 changes state, the trailing edge at Q causes a positive clock pulse to be given to shift register IC2 via N16 (provided the second input of this NOR gate is 0). Simultaneously, input A of MMV2 goes high which prevents the point counter and lamp being triggered. Monostable MMV2 is also rendered inoperative when switch S4b is open. The two 4-bit binary counters type 74LS93, apart from indicators, also function as control elements. Outputs C and D of tsk counter IC4 provide a logic 1 to the inputs of NAND gate N10 after the twelfth input (binary 1100). The output of N10 is then 0 which keeps both monostables inactive until pressing reset switch S5 enables the acceptance of a fresh program.

A further important function of counter IC4, together with NAND gate N9 and NOR gate N15, is to prevent once per program, in counter position 0110 (sixth input), the provision of a clock pulse to the shift register. In this situation both inputs of N15 are 0, one input of NOR gate N16 is therefore 1, and the clock pulse for IC2 is blocked.

We now see how an 8-bit shift register may function as a 8 x 12-bit memory: inputs A and B are connected to output Q via switch S4a and IC2 then functions as a ring register. Because the clock pulse is absent at the 6th input, the contents of the register are run through after the 9th input: the last and first three steps in a program are therefore identical. The memory is thus shifted by three bits every program and the original line sequence does not recur until after eight through-runs.

The output of NAND gate N11 is normally logic 1 and only becomes 0 when the user has reached the 12th input, that is, when the point counter indicates 1100. The output of NAND gate N12 is then 1 which actuates oscillator N29 and this causes lamp Lal to flash at a frequency of about 2 Hz via inverter N17 and driver stage T1. To keep the switch-on current of the lamp low, it is pre-heated by a quiescent cur-

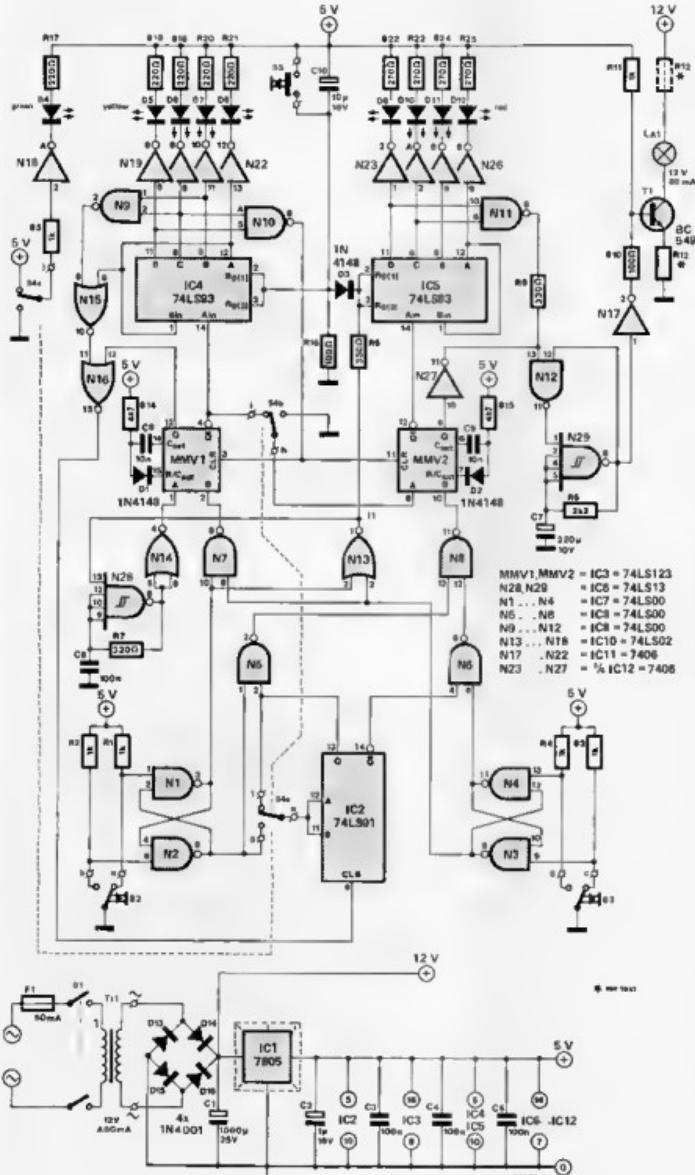


Table 1.

Program A

1. L-R R-L-R-L-L-R-L-L-R-A
 2. L-R-L-R-L-L-L-R-R-L-R-L
 3. R-L-L-R-L-R-L-L-R-L-L
 4. R-R-L-R-L-R-L-L-R-L-R
 5. R-L-R-L-L-R-R-L-R-L-R
 6. L-L-R-R-L-R-L-R-L-L-R
 7. R-L-R-L-R-L-L-L-R-R-L-R
 8. L-R-L-L-R-R-L-R-L-R-L-R
 1. L-R R-L-R-L-L-R-L-L-R-A

Program B

1. R-L-R-A-R-L-R R L-L-R-L-R
 2. R-L-R-L-L-R-A-R-L-R-L-R
 3. L-L-R-L-R R R-L-R-L-L-R
 4. L-R-R-L-R-L-L-R-L-R-R
 5. L-R-L-L-R-L-L-R-A-L-L-R
 6. L-R-L-R A R L-L-R-L-L-R-L
 7. R-R-L-R-L-L-L-R-L-R-L
 - 8 R L-L R-L-R-A-R-L-R-L-R
 9. R-L-R-A-L R-A-L-L-R-L-R

Program C

1. L-L-R-R-L-A-R-R-L-L-L-R
 2. R L-R-R-L-L-L-L-R-R-L-R
 3. R-L-L-L-R-A-R-L-A-R-L-L
 4. L-R-R-L-R-R-R-L-L-L-R-R
 5. L-R-R-L-L-L-L-R-A-L-L-R
 6. L-L-L-R-A-L-L-A-R-L-L-L
 7. R-A-R-L-A-R-L-L-L-R-A-L
 8. R-R-L-L-L-R-A-R-L-A-R-L
 1. L-L-R-A-L-A-R-L-L-L-R

Table 1. Three examples of the thirty-eight possible program blocks.

Figure 1. The circuit diagram looks rather more complex than it is. As everything is digital, no calibration is necessary.

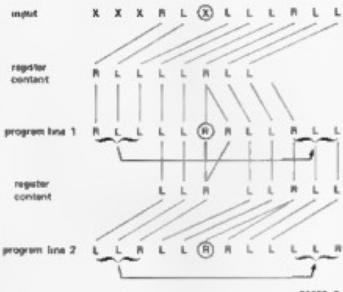


Figure 2. An example of a suitable program. The top line shows the key inputs necessary for loading the ring register. The second line shows the contents of the ring register after loading (1st cycle). The third line gives the correct answers to the first cycle of twelve questions. The fourth line shows the contents of the ring register after loading (2nd cycle). The fifth line gives the correct answers to the second cycle of twelve questions.

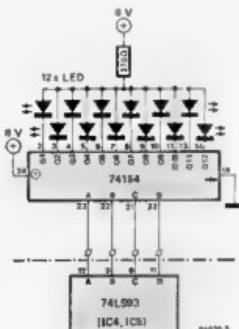


Figure 3. An alternative for the indication of the number of the questions and the points score. This circuit must, of course, be built twice: one for IC4 and one for IC5. Connecting the LEDs in bars above or beside one another makes the indication clear even for children.

rent provided by R_{11} . This current is kept at about 25 per cent of the operating current by emitter resistor R_{13} . The value of R_{13} is thus determined by the operating current of the lamp used: about $27\ \Omega$ for 30 mA , $10\ \Omega$ for 80 mA , and 4Ω for 160 mA .

Oscillator N28 is normally blocked by the logic 0 at the output of NOR gate N13: its output is therefore high and this causes NOR gate N14 to keep input A of MMVI low. When both input switches are pressed, the output of N13 goes high, and the oscillator causes the task counter to count to the next '12', and IC2 to shift to the next program line, via MMVI. To prevent unjustified points being awarded, the reset inputs of IC5 are connected to the output of N13, and in the above situation are logic 1. The normal reset pulse is derived from diode D3.

construction

We have chosen coloured LEDs for the binary indication, which are inexpensive and look good. As an aside, they quickly

teach you the binary coding if you are not already familiar with that.* The best are miniature LEDs (may be obtainable in an array) which can be connected directly to the +5 V line via a biasing resistor. Make sure that the LEDs all have the same brightness before soldering them in. As regards the power supply, no more need be said than that the maximum current consumption is about 250 mA . Voltage regular IC1 must be fitted onto a heat sink.

The circuit is best built into a case which is suitable for use on a desk or table top.

programming

It is not particularly difficult to devise your own program. The circuit should first be reset and switch S4 closed so that LED D4 lights. You then choose an arbitrary sequence of eight L/R instructions for shift register IC2, for instance, R-L-L-L-R-L-L, and extend this arbitrarily with four Xs. Your input may then look like that shown in figure 2.

Instruction 6 (R) is not written in the first program line, because the clock pulse for IC2 is then suppressed. To avoid this information getting lost, instruction 6 must be repeated. The first three inputs (R-L-L) are omitted from the ring register but are added at the back (second register contents). This procession is repeated until after eight runs the original input line recurs.

In this method of programming shifts occur and the program lines and the register contents are therefore not identical. As the program runs as a cycle, it may be read from any arbitrary position by selecting a line of the register contents and accepting the following line as the first program line. In this way it is possible to obtain eight program blocks from one (as, for instance, block A in Table 1), and by interchanging L and R, even sixteen. To start with, this will certainly be sufficient. After a program has been written, S4 should be set to its original position, and the circuit reset by means of S5.

*None the less, especially for younger users, figure 3 shows an alternative way of indicating the number of the question and the points scored.

Digi-Course II

Chapter 1

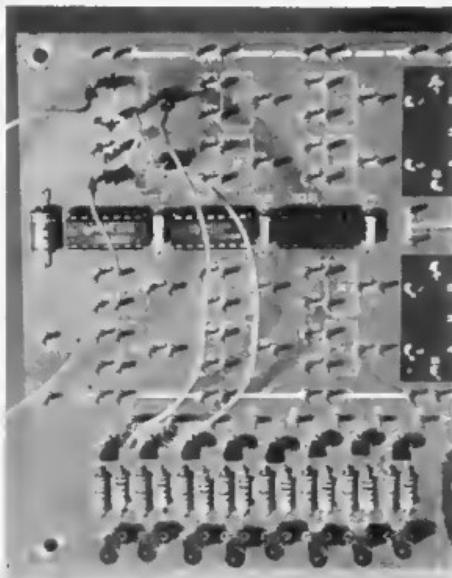
In the six chapters of our Digi-Course covered so far, we have learnt about basic gates. These basic gates had fixed relations between inputs and outputs, defined by their individual truth tables.

From this issue, we start the second phase of our Digi-Course. In this part we shall learn about sequential logic circuits. The term sequential means that the relations of the outputs are not only dependant on the present input conditions but depend also on the previous conditions of inputs and outputs. The word "sequential" is derived from the Latin word *sequentia* which means succession.

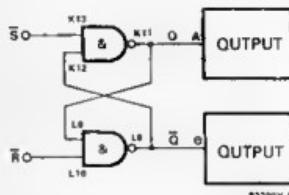
A simple example of sequential operation of a device is the table lamp with a push button switch. When you push the switch the lamp lights. Push the same switch again and the lamp goes off. The action is same but the results are totally different. This example illustrates the meaning of sequential logic. If we consider the push button switch as the input and lamp as the output, we can see that for an input condition—"push the switch" the output condition—"lamp lights" is either true or false depending on the previous condition of the output.

FLIP FLOP

The first sequential logic circuit that we shall see is the flip flop. This consists of two NAND gates connected together as shown in figure 1.



1



The truth table for this circuit is not as simple as the truth tables we have so far seen for the static logic gates.

Table 1.

S	R	Q	Q̄
0	0	t	t
0	1	t	0
1	0	0	t
1	1	0/t	1/0

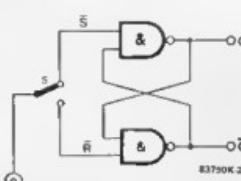
This truth table will have input-output relations which are time dependent. The truth table for the circuit of figure 1 is given in table 1. It has three input combination which have definite output combinations each. The last input combination, where both the inputs are "1", has no definite output combination, it depends on the previous conditions on outputs Q and Q̄, the previous condition of Q and Q̄ is retained when R & S are both "1". The flip flop inputs are marked S and R̄ because they are called Set and Reset inputs to the circuit, the dashes above S and R indicate that the active value of these inputs is "0". The dash is the sign of logical reversal. The outputs are called Q and Q̄ but the latter Q here has no special significance.

The flip flops are practically used as logic switches. The circuit of figure 1 is in a simplified form given for understanding the basic principle behind the operation of flip flops.

In the case of practical flip flops the two outputs Q and Q̄ are always opposite of each other. The term "Set" means setting the output Q to "1" and "Reset" means resetting it to "0".

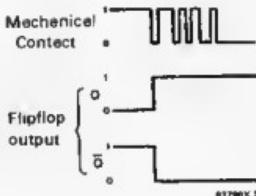
The flip flops are frequently used in practical applications alongwith mechanical switches and relays.

2



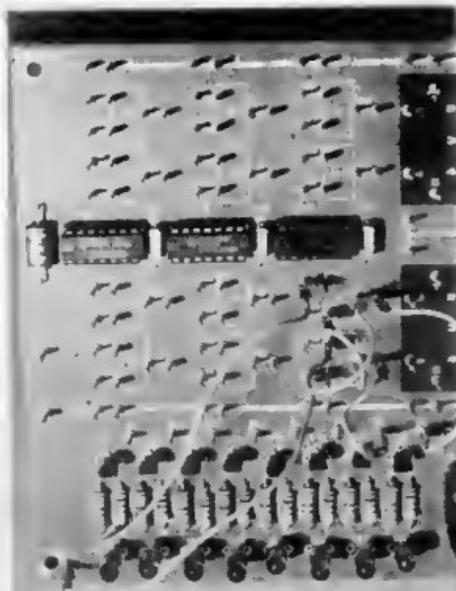
Logically the functioning of a mechanical contact and a flip flop is same. However the transition from 0 to 1 or 1 to 0 in a mechanical contact is not as smooth as in case of a flip flop. Figure 3 shows how a mechanical contact can "chatter" for a fraction of a second before reaching steady state.

3

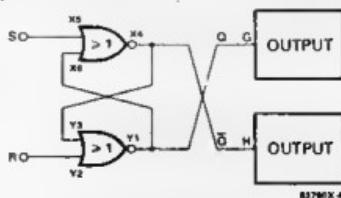


The flip flop switches smoothly just by giving a pulse to the set or reset input; and has no transient noise like a mechanical contact. This is a very critical requirement in case of sensitive measuring circuits which can pick up all the transient noise of a mechanical contact and cause malfunctioning of the system.

Similar to the flip flop of figure 1 constructed using two NAND gates, we can also connect two NOR gates to obtain a flip flop.



4



However, this circuit has a different truth table compared to the truth table of the circuit shown in figure 1. This is natural as we have used NOR gates in place of NAND gates. The input condition when both R & S are "D" retains the previous conditions of Q and Q-bar.

Table 2.

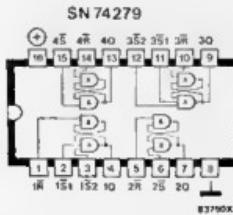
S	R	Q	\bar{Q}
0	0	0/1	1/0
0	t	0	t
t	0	1	0
t	1	0	0

The S and R inputs have no dash shown above them here, because the set or reset is done by a "1" and not by a "0" as in the previous circuit.

These two circuits can be connected on the Digilex Board and the input output relations can be studied by giving suitable input values of "0" and "1". Remember that an open, unconnected input on any gate will behave as if it was on "1".

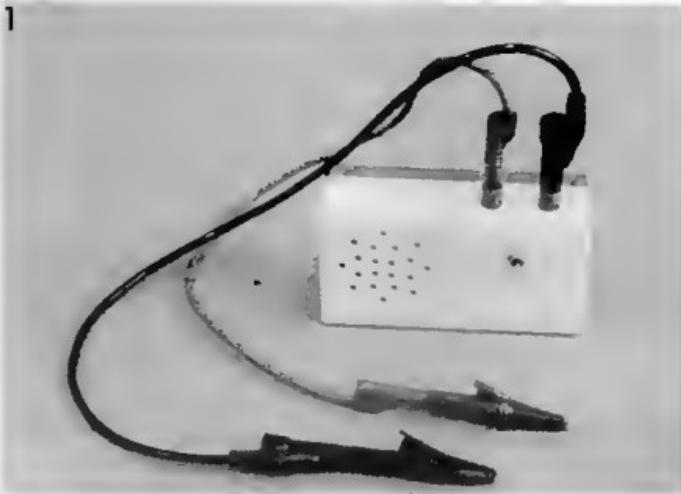
As the inputs of this type of flip flop are for Reset/Set function, this flip flop is called the RS-Flipflop. Four of such RS flip flops are available in a single IC, 74279. Two of these flipflops have one of their NAND gate with 3 inputs. The schematic diagram for this IC is shown in figure 5 below.

5



Audible Continuity Tester

1



Testing continuity with a multimeter poses one problem, you can't look at the probe tips and at the meter at the same time. So when you are looking at the meter you are not sure if the probe tips are touching the right point.

This month, selex brings you a continuity tester which does not divide your attention. A continuity tester which beeps to tell you if there is a continuity between the two points you are touching with the probe tips.

This can be used for testing continuity in almost everything that conducts electricity.

The Circuit

The basic circuit of the audible continuity tester is shown in figure 2

Transistors T1 and T2 form the audio oscillator, the so called astable multivibrator. T3 amplifies the signal so that it can drive the speaker. Test clips are connected between points A and B. When the test clips touch a conductive path, current flows through them and through the path being tested for continuity. When the current flows, the multivibrator gets power supply and produces the audio signal which can be heard through the speaker. Conductive paths having resistances upto about 100Ω can be tested with this circuit.

The Multivibrator

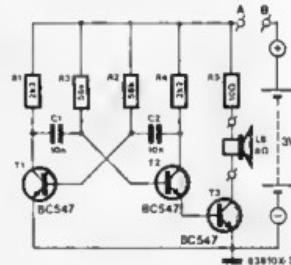
The astable multivibrator works as follows :

Transistor T1 and T2 are connected in such a way that only one of them can conduct at a time. When we switch on the supply, which one will be conducting, is unpredictable.

Assuming that T1 is conducting when the circuit gets the supply, the collector voltage of T1 will be low.

Capacitor C1 ensures that initially the base voltage of T2 is low and hence T2 is cut off (not conducting). However

2



3

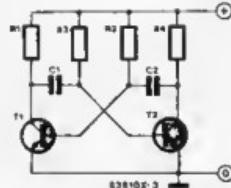


Figure 1.
The audible continuity tester.

Figure 2.
Circuit diagram of the audible continuity tester.

Figure 3.
The basic multivibrator circuit.

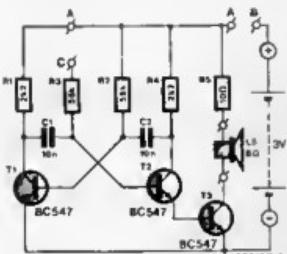
the current flowing through R3 charges the capacitor C1. As the charge on C1 builds up to such a level that the base voltage of T2 exceeds 0.7V, T2 starts conducting due to this forward bias on its base. As a result of this, the collector voltage of T2 suddenly drops, and due to capacitor C2 the base voltage of T1 suddenly drops. This low voltage on base of T1 brings it out of conduction and it is now cut off. This time resistor R2 charges capacitor C2 till the voltage on base of T1 again rises to about 0.7V, and T1 again starts conducting. This cycle continues so long as the power supply is connected.

If we see the emitter current of T2 during this process, we find that it repeatedly becomes low and high at a frequency determined by the values of C1, C2, R3, R2. In our circuit, the frequency of oscillation is around 1000 cycles per second (1 KHz). The oscillating emitter current of T2 causes T3 to pass an oscillating current through its collector circuit which contains the speaker. This oscillating current through the speaker produces a sound of 1KHz frequency which we hear as continuous tone. If the supply is given to the circuit momentarily, it produces a beep sound.

As we have already seen, the circuit of figure 2 can test conductive paths having resistance only upto 100Ω . For testing conductive paths with high resistances, the circuit needs to be modified as shown in figure 5.

This modified circuit will work with contact resistances even upto $1\text{ M}\Omega$. If you want a tester with both facilities, use a three position switch as shown in figure 5.

4



Construction

The entire circuit can be assembled on a small standard PCB as per the layout shown in figure 6. Avoid using bare copper wires for jumpers as it may create short circuits unintentionally.

Start soldering the passive components first, then solder the transistor.

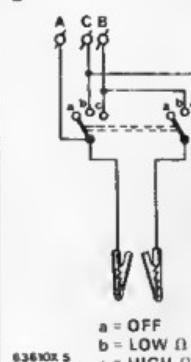
The PCB and speaker can be fixed in a small case as shown in the photograph. Speaker can be directly pasted with adhesive. (Be careful not to drop any adhesive on the cone of the speaker.)

Soldering wires to banana sockets requires patience, because the area being larger, it takes quite some time to get hot enough for a good soldered joint.

Figure 4.
The modified circuit of tester for high resistance paths.

Figure 5.
3-Position switch connections for the High-Low Ohms combined version.

5



38610X5

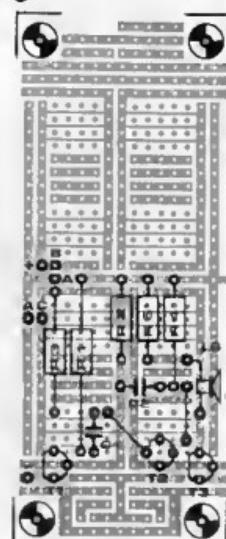
Component List

R1, R4 = $2.2\text{ k}\Omega$
 R2, R3 = $56\text{ k}\Omega$
 R5 = $10\ \Omega$
 C1, C2 = 10 nF
 T1, T2, T3 - BC 547
 LS = B10 Loudspeaker (0.2 W)

Other parts

1 Battery holder for 2 penlight cells.
 2 Penlight cells.
 1 Suitable Case.
 2 Banana Sockets.
 2 Banana plugs.
 2 Crocodile Clips.
 1 3-position double pole switch.
 1 Standard PCB
 and suitable length of insulated flexible wire.

6



Potentiometers

In the last issue we have studied the properties of Resistor combinations - parallel and series. We have seen how two resistors connected in series and the combination across a voltage source behaves. The two resistors R1 and R2 divide the voltage of the source between themselves in such a way that current through both of them remains same, as they are connected in series. The voltage across each of them is simply the product of the current and the resistance value in Ohms.

1

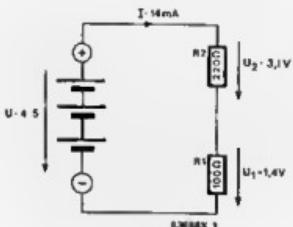


Figure 1 shows a practical circuit which has a series combination of two resistors R1 and R2 across a voltage source. The resistance values are 100Ω and 220Ω (approximately) this gives a ratio of $R1/(R1+R2)$ as 1/3.

This means that the voltage U_1 across the resistor R1 will be about 1/3 of the total battery voltage, the exact value being 1.4V. Assuming that this is the voltage we wanted to derive for some practical application from the 4.5V battery, it means that the remaining 2/3 voltage which appears across R2 will be wasted as heat dissipated by heating up the resistance R2.

The voltage dividers using resistors like this are the simplest means of obtaining the required voltages from a larger source. However, as we have seen it is the most inefficient method of doing so. Fortunately, as the total energy consumption of electronic circuits is generally very small, the inefficiency of the voltage dividers can be overlooked in favour of the simplicity they present.

For AC voltages, transformers are the most efficient voltage dividers, and series combinations of resistors are seldom used.

Potentiometers

The voltage divider in the most widely used form is a "Potentiometer", generally referred to as "Pot" for simplicity. A potentiometer is not just a voltage divider similar to the one seen before, but it is a variable voltage divider. The $R1/R2$ ratio is variable, keeping $(R1+R2)$ constant. The specified value of a potentiometer is this sum $(R1 + R2)$; which in fact is a single resistance end not a combination of R1 & R2. The resistance is either made of a track of resistive material or may consist

2

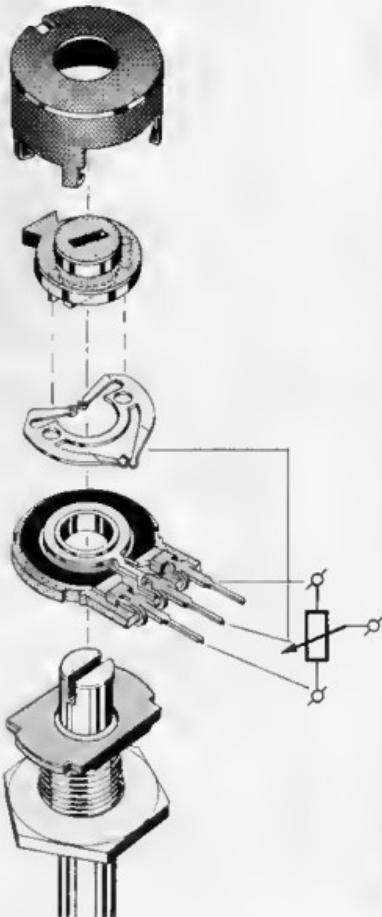


Figure 1

The current in the circuit flows through both R1 & R2, developing voltage drop proportional to their individual values. The resistors thus divide the battery voltage.

Figure 2.

The slider contact of the potentiometer varies the individual values of R1 and R2 such that $R1 + R2$ remains constant equal to the potentiometer's total resistance value. The ratio $R1/(R1+R2)$ thus becomes variable.

of a winding of resistance wire. A sliding contact moves over this resistance, dividing the total resistance into two parts R_1 and R_2 , and the ratio $R_1/(R_1+R_2)$ depends on the position where the sliding contact is positioned. $R_1/(R_1+R_2)$ can be varied from 0 to 1 over the full range of movement of the sliding contacts. $R_1/(R_1+R_2)$ is called the voltage divider ratio which gives us the voltage at the contact point of the sliding contact variable from 0 to the full source voltage.

A typical application of the potentiometers is in volume controls. Figure 4 shows a schematic representation of how the potentiometer is used in volume control application. The potentiometer is located between the preamplifier and the power amplifier. An amplifier is seldom used at its full capacity because of the distortions it introduces. The power amplifier is designed for a higher output than what is required, and to set the volume at the desired level the potentiometer is used as a voltage divider across the output voltage of the preamplifier. The input to the power amplifier is taken from the sliding contact of the potentiometer, so that the voltage at the input of power amplifier is decided by the voltage divider ratio $R_1/(R_1 + R_2)$.

In the lowest position of the potentiometer, the ratio is zero and no voltage is passed on to the power amplifier. All the output from the preamplifier is wasted as heat in the potentiometer.

The input of the power amplifier is effectively shorted to ground through the slider contact.

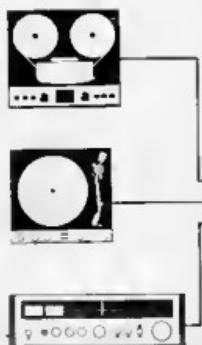
In the highest position the potentiometer has the voltage divider ratio of 1 and the full output of the preamplifier is fed to the power amplifier.

The input of the power amplifier is effectively shorted to the output of the preamplifier through the sliding contact.

The control over the volume is thus right from zero volume to full volume.

It is not always necessary that a potentiometer be always used as a voltage divider. Figure 5 shows another application for the potentiometer. By leaving one end of the potentiometer resistance open or by connecting it to the sliding contact, we can use a potentiometer as a variable resistor.

4



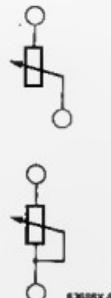
Volume control

Power amplifier.



8368X-4

5



8368X-5

Formulae

For the sake of completeness, let us see how the voltage divider calculations are done. We shall take the circuit of figure 1 as an example.

The total resistance of the voltage divider is :

$$\begin{aligned} R_g &= R_1 + R_2 \\ &= 100 \Omega + 220 \Omega \\ &= 320 \Omega \end{aligned}$$

The current flowing through the $(R_1 + R_2)$ combination, known as the idle current is :

$$\begin{aligned} I &= U/R_g \\ &= 4.5V/320\Omega \\ &= 14mA \end{aligned}$$

The voltage drop across individual resistors R_1 and R_2 are .

$$\begin{aligned} U_1 &= R_1 \times I \\ &= 100\Omega \times 14mA \\ &= 1.4V \end{aligned}$$

$$\begin{aligned} U_2 &= R_2 \times I \\ &= 220\Omega \times 14mA \\ &= 3.1V \end{aligned}$$

The voltage across R_1 , which is of interest to us, can be also be calculated by using the following relation:

$$U_1 = U \times R_1 / (R_1 + R_2)$$

The fraction $R_1 / (R_1 + R_2)$ is the voltage divider ratio.

Figure 4.
Schematic diagram of a Hi-Fi amplifier. The volume is controlled by the potentiometer sliding contact position.

Figure 5

Potentiometer used as a variable resistor.

Polarity Tester



As you might have correctly guessed, a polarity tester can be constructed by connecting a diode and a lamp in series. When a voltage is applied as shown in figure 1, the lamp will glow. If the polarity is reversed the lamp will not glow (Figure 1).

Even though this circuit is very simple to construct and use, unfortunately it has a very important disadvantage. It functions only if the voltage is sufficient to light up the bulb. With a small voltage, less than the value required by the bulb, the circuit will not function with whatever polarity you connect.

This flaw can be overcome, with a little help of electronics. Figure 2 shows a modified circuit of our simple polarity tester.

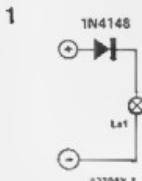
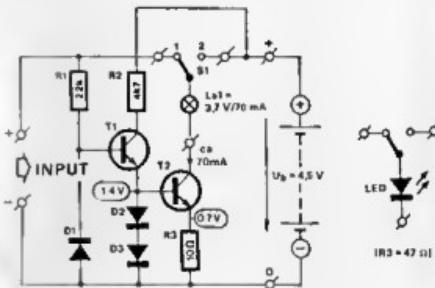


Figure 1.
The lamp glows if the polarity of the test voltage is correct.

2



D1...D3 = 1N4148
T1 T2 = BC547B

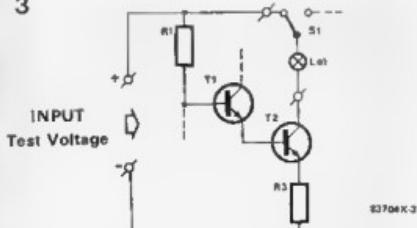
83704X 2

Figure 2.
Complete circuit diagram of the Polarity Tester.

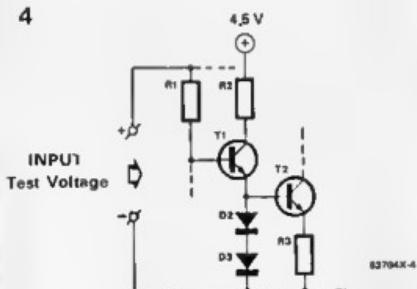
The basic circuit of the polarity tester consists of the lamp L 1 the transistor T 2 and resistor R3. The transistor T2 works as an electronic switch for turning the lamp ON and OFF. Transistor T1 controls the operation of T2. How this happens is illustrated in Figure 3. It can be seen that when the Base-Emitter junction of transistor T1 is forward biased, it supplies base current to transistor T2. At the same time the collector current of T1 flows through R2. The combination of base and collector current of T1 leaves the emitter of T1 and is again distributed between the base of T2 and diodes D2 and D3. As the diodes are forward biased, they conduct. This gives rise to a voltage of $(0.7 + 0.7) = 1.4$ Volts at the base of T2. The base-emitter junction of T2 is also forward biased and produces a voltage of 0.7V. Effectively the voltage across R3 is 0.7V, independent of other voltages in the circuit. From our knowledge of Ohm's Law we can derive the emitter current of T2 to be $70\text{mA } I = V/R = 0.7V/10 \Omega = 70\text{mA}$

At this point you will recollect that we have already seen a similar circuit - the constant current source. The base current being small compared to the emitter current, we can consider the emitter current to be almost equal to the collector current. Thus the current passing through the lamp L1 is always 70mA, provided that T1 provides the base current for T2. This is possible when the voltage connected at the test terminals is of the correct polarity. In case a reverse voltage is applied, T1 does not supply the base current for T2 and the lamp does not glow.

3

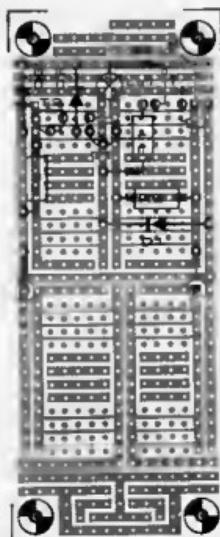


4



With a reverse voltage at the test terminals, diode D1 conducts and provides protection to the remaining circuit from damage due to reverse polarity.

5



In case the test voltage is too low to drive a lamp, as we have seen before, the switch S1 can be thrown to position 2 so that the 4.5V battery supplies the current for the lamp. The current drawn from the test voltage in this case will be just about 5 microamperes (1 microampere is one millionth of an ampere).

To reduce the current drain from the 4.5V battery, and LED can be used in place of the lamp. This requires the resistor R3 to be changed to 47Ω instead of 10Ω.

Construction :

The circuit is very simple to construct, and if it is constructed properly as per the layout shown in figure 5 it should work at the first attempt.

The usual precautions must be taken and the terminals of diodes and transistors must be correctly identified to avoid wrong connections.

A separate switch for the battery is not provided, as the idle current is not more than 1 micro ampere.

The polarity tester can be used for voltage from 3V to 45V, and the lower lever of range can be brought down to 1.5V by using an LED in place of lamp and using a 9V battery in place of the 4.5V battery.

Component List :

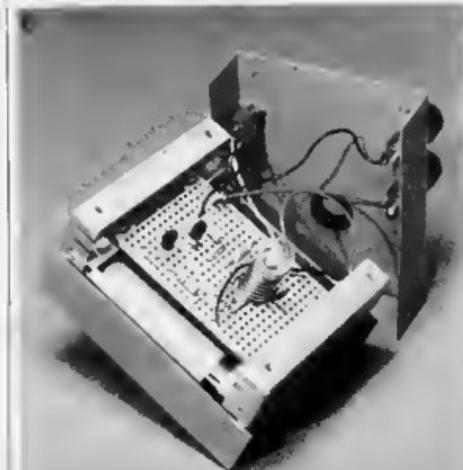
R1 = 22 kΩ
 R2 = 4.7 kΩ
 R3 = 10Ω
 O1, D2, D3 = 1N 4148
 T1, T2 = BC 547B/BC147B
 La1 = 3.7V/70mA Bulb
 S1 = SPDT switch

Other parts :

1 Standard PCB
 1 4.5V (or 9V) Battery
 1 Bulb socket
 1 suitable cabinet

Changes for LED version :

1 LED instead of Lamp La1
 R3 = 47Ω instead of 10Ω



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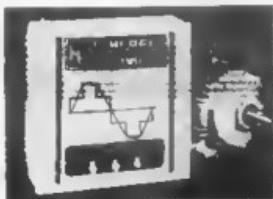
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